Design Example Report

Title	***65 W Isolated Flyback Power Supply Using InnoSwitch™3-EP PowiGaN™ INN3679C-H606 and MIN1072M***
Specification	90 VAC – 265 VAC Input; 20 V, 3.25 A Output
Application	Adapters
Author	Applications Engineering Department
Document Number	DER-726
Date	March 23, 2021
Revision	1.0

Summary and Features

- 65 W output power capability at 20 V
- >92% average efficiency at nominal AC inputs
- <50 mW no-load input power at nominal AC inputs
- Integrate protection and reliability features
  - Output short-circuit
  - Line and output OVP
  - Over-temperature shutdown
- Synchronous rectification for higher efficiency
- Input voltage monitor with accurate brown-in/brown-out protection
- Meets EN55022 and CISPR-22 Class B conducted EMI
- Meets IEC 1.0 kV differential surge
- ±16 kV ESD Class B

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes an isolated flyback converter designed to provide a 20 V 3.25 A output from a wide input voltage range of 90 VAC to 265 VAC. This power supply utilizes the INN3679C-H606 from the InnoSwitch3-EP family of IC's with the input capacitor volume-reduction capabilities of the MinE-CAP IC.

This document contains the complete power supply specifications, bill of materials, transformer construction, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.

Figure 1 – Prototype Top View

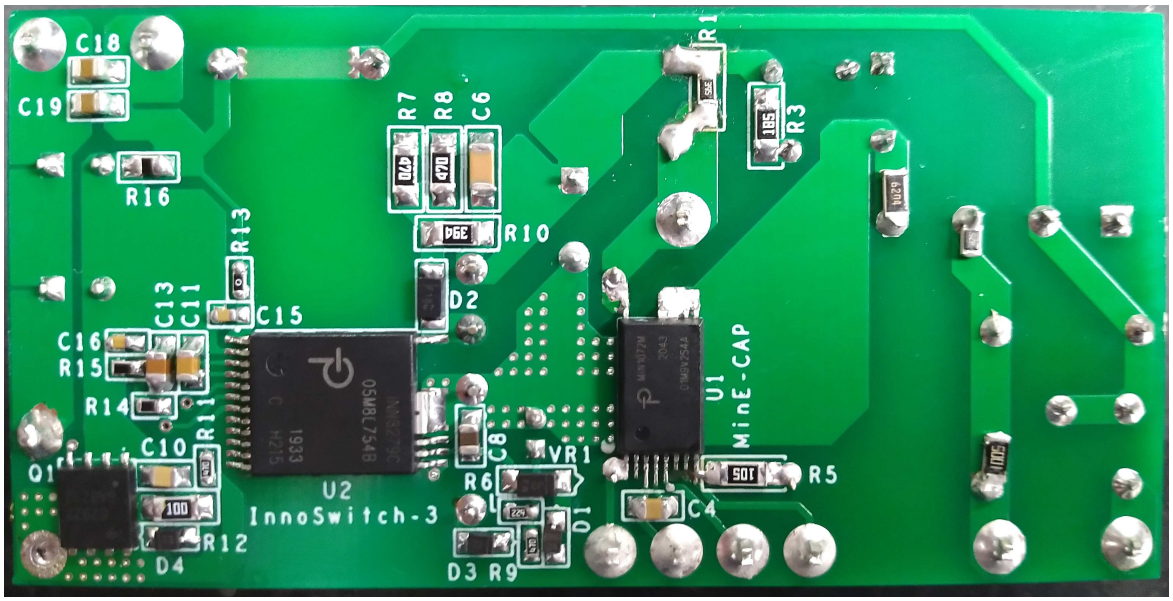

Figure 2 – Prototype Bottom View

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				<50	mW	
Output						
Output Voltage	V_{OUT}	19	20	21	V	± 5%
Output Ripple Voltage	V_{RIPPLE}			450	mV	20 MHz Bandwidth.
Output Current	I_{OUT}			3.25	A	
Total Output Power						
Continuous Output Power	P_{OUT}			65	W	
Efficiency						
Full Load @ 115 VAC	η	92			%	
Full Load @ 230 VAC	η	93			%	Measured at P_{OUT} 25 °C.
Average @ 115 VAC	η	92			%	
Average @ 230 VAC	η	93			%	
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Surge (Differential)				1	kV	1.2/50 μs Surge, IEC 61000-4-5, Impedance: 2 Ω
ESD – Air Discharge				±16	kV	
ESD – Contact Discharge				±8	kV	
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

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3 **Schematic**

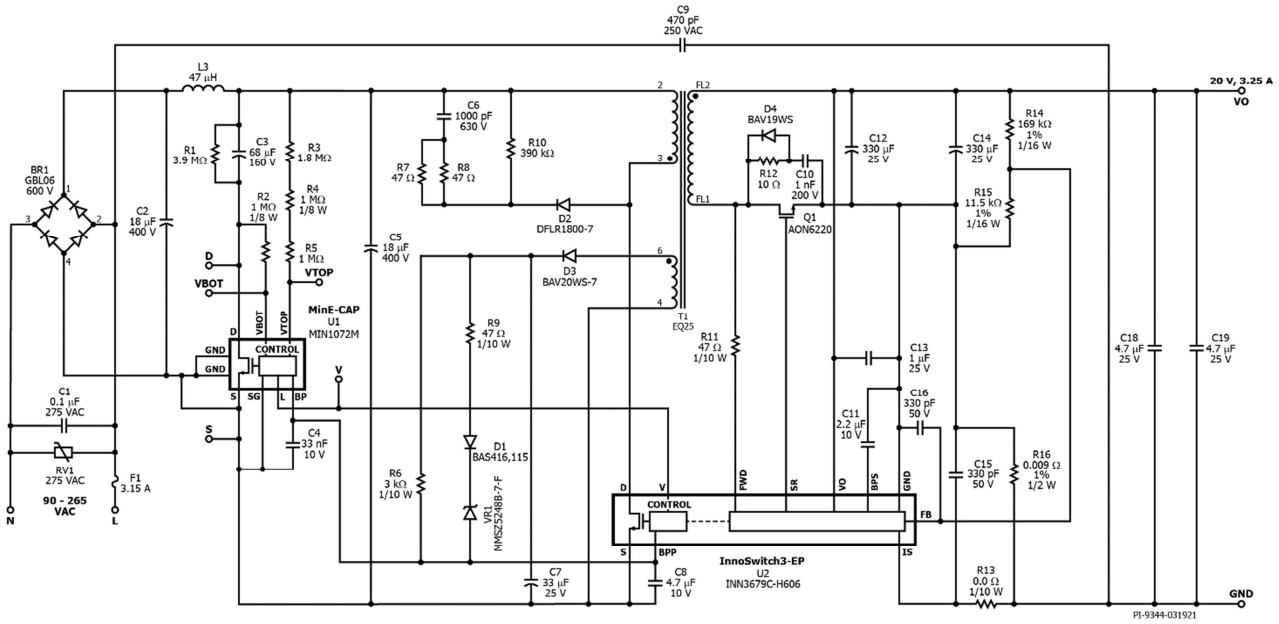

Figure 3 – Schematic.

4 Circuit Description

The InnoSwitch3-EP IC combines primary, secondary and feedback circuits in a single surface mounted off-line flyback switcher IC. The IC incorporates the primary MOSFET, the primary-side controller, the secondary-side controller for synchronous rectification, and the Fluxlink™ technology which eliminates the optocoupler needed on a secondary-sensed feedback system.

4.1 *Input Rectifier and Filter*

Fuse F1 isolates the circuit and provides protection from component failure. Bridge rectifier BR1 converts the AC line voltage into the DC voltage seen across the input filter network. EMI filtering is provided by the X capacitor C1 and mainly by the pi filter combination of C2, L3, and C5. Capacitor C3 further bolsters EMI suppression at lower input voltages.

4.2 *MinE-CAP MIN1072M*

The MinE-CAP U1 basically connects the low voltage capacitor (LV cap) C3 when the input voltage is low and disconnects when the input voltage is high. By connecting the L pin to the V pin of the Innoswitch3-EP IC, the MinE-CAP IC provides the AC input information to the InnoSwitch3-EP IC for undervoltage and overvoltage levels. The MinE-CAP IC also reduces inrush currents by way of controlled charging of the LV caps thereby eliminating the need for inrush NTC's. Information needed for proper control is provided by the network of sense resistors R2, R3, R4, and R5 via the voltages measured on the V_{TOP} and V_{BOT} pins. R1 is a bleeder resistor used to help regulate the voltage across the LV cap.

4.3 *InnoSwitch3-EP Primary-Side*

The primary side of INN3679C combines a high-voltage power MOSFET and the primary side controller into a low cost monolithic IC.

When AC is first applied, an internal current source connected to the DRAIN (D) pin charges C8 to power the controller inside the IC. During steady-state, the device controller will now be powered via a bias winding through the current limiting resistor R6 to minimize losses.

The power transformer T1 is designed for a flyback topology power supply. The start winding of the transformer is connected to the DRAIN pin of the MOSFET inside the INN3679C, while the end of the winding is connected to the rectified DC bus. A low cost RCD clamp consisting of diode D2, capacitor C6, and resistors R7, R8, and R10 limits to acceptable levels the effects of leakage energy generated by the transformer leakage inductance.

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4.4 *InnoSwitch3-EP Secondary-Side*

The secondary-side of INN3679C provides output voltage sensing, output current sensing, and internal gate driver for a synchronous rectifier (SR) MOSFET. The secondary-side is powered by an internal 4.4 V regulator which draws current from either VOUT or the current-limited FWD pin via R11. Its output is connected to an external decoupling capacitor C11, also referred to as BPS capacitor.

The FWD pin also provides negative edge detection by sensing the transformer's secondary pin through resistor R11. The voltage sensed by the FWD pin is used for both the primary-secondary handshake at start-up, and for timing the turn-on instant of the SR FET Q1. This ensures quasi-resonant operation when operating at discontinuous conduction mode (DCM).

The SR FET Q1 is driven by the SR pin of U2. The RCD snubber consisting of R12, C10, and D4 limits the drain to source voltage spike across the SR FET.

The feedback network comprised of resistors R14 and R15, and capacitor C16 is connected between the output voltage and secondary ground. The sensed voltage across R15 is connected to the FB pin. The external current sense resistor R16 connected between the ISENSE and SECONDARY GROUND pins sets the maximum output current limit.

Low ESR capacitors C12 and C14 provides output filtering. Output voltage ripple is further reduced by the ceramic capacitors C18 and C19.

5 PCB Layout

PCB material: FR4, Thickness: 1.6 mm, Copper: 2 layers, 2 oz.

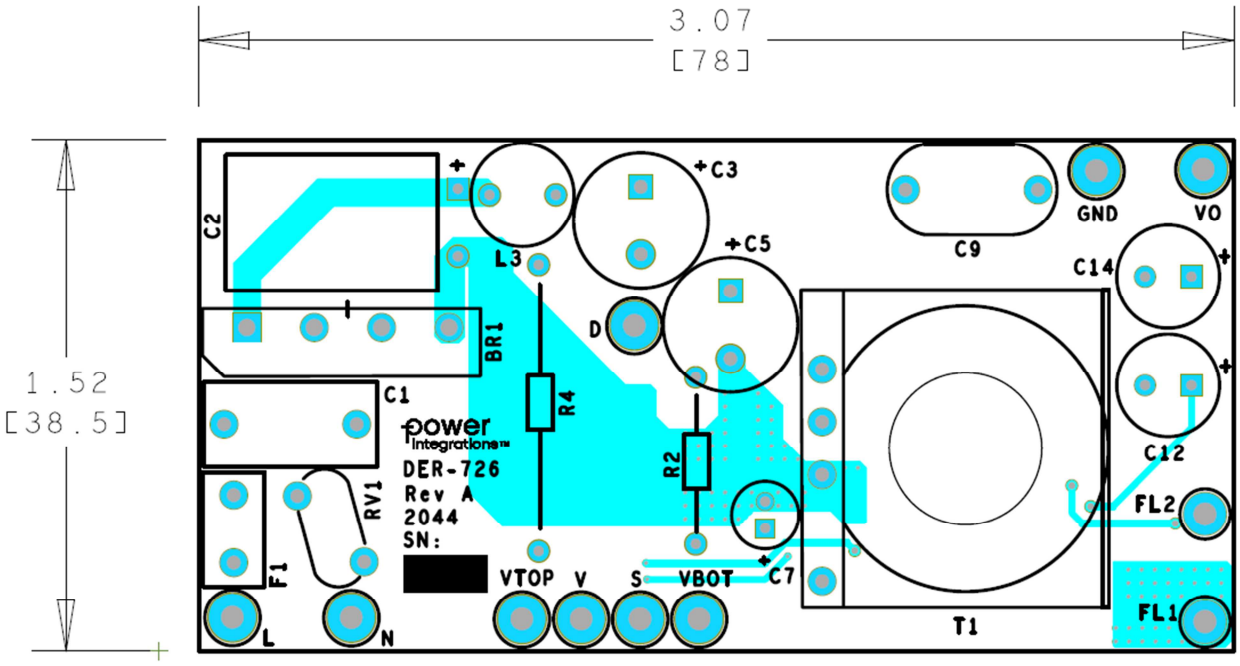

Figure 4 – Populated Circuit Board, Top View.

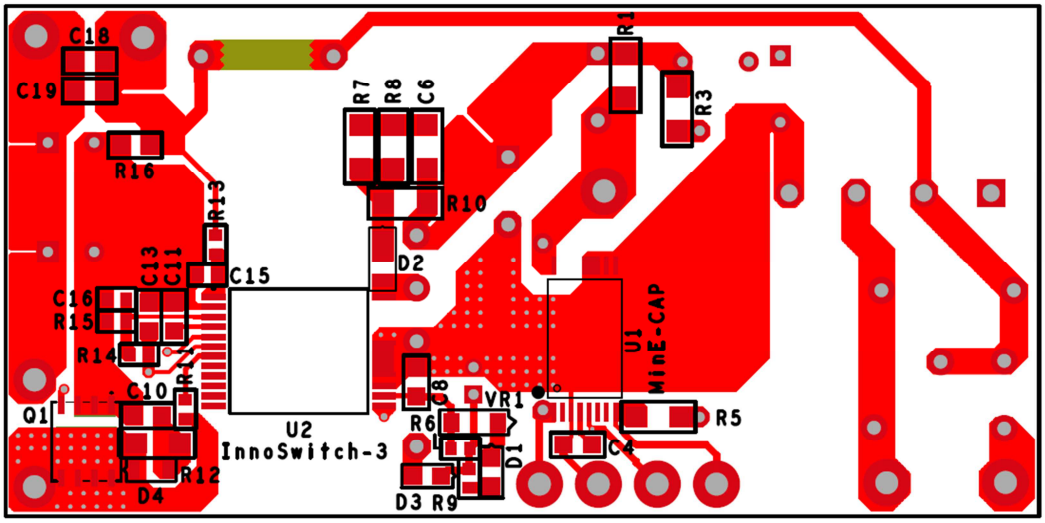

Figure 5 – Populated Circuit Board, Bottom View.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	DIODE BRIDGE 600 V 4 A GB	GBL06	Genesic Semi
2	1	C1	0.1 µF Film 275V Polypropylene (PP), Metallized Radial	890324023023	Würth
3	2	C2, C5	18 µF, 20%, 400 V, Electrolytic, Gen. Purpose, (10 x 16 mm), 2000 Hrs @ 105°C	400AX18MEFC10X16	Rubycon
4	1	C3	68 µF,20%, 160 V, Electrolytic, Gen. Purpose, (10 x 20), 10000 Hr @ 105C	160BXW68MEFR10X20	Rubycon
5	1	C4	33 nF, 0.033 µF,10 V, Ceramic, X7R, 0805	0805ZC333KAT2A	AVX
6	1	C6	1000 pF, 630 V, Ceramic, X7R, 1206	C1206C102KBRACTU	Kemet
7	1	C7	33 µF, ±20%, 25 V, Electrolytic, -55°C ~ 105°C, 2000 Hrs @ 105°C, Gen. Purpose, (5 x 11)	UPW1E330MDD	Nichicon
8	1	C8	4.7 µF, 10 V, Ceramic, X5R, 0805	C0805C475K8PACTU	Kemet
9	1	C9	470 pF, 250 VAC, Film, X1Y1	DE1B3KX471KN4AN01F	Murata
10	1	C10	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
11	1	C11	2.2 µF, 10 V, Ceramic, X7R, 0805	C0805C225M8RACTU	Kemet
12	2	C12, C14	330 µF, ±20%, 25 V, Al Organic Polymer, Gen. Purpose, Can, 18 mΩ, 2000 Hrs @ 105°C, (8 mm x 13 mm	A750KS337M1EAAE018	KEMET
13	1	C13	1 µF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
14	2	C15, C16	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
15	2	C18, C19	4.7 µF ±10%, 25 V, X7R, 0805, -55°C ~ 125°C	TMK212AB7475KG-T	Taiyo Yuden
16	1	D1	Diode, Low Leakage, 85 V, 200 mA, SOD323	BAS416,115	NXP Semi
17	1	D2	800 V, 1 A, Rectifier, POWERDI123	DFLR1800-7	Diodes Inc
18	1	D3	200 V, 200 mW, Diode, SOD323	BAV20WS-7-F	ON Semi
19	1	D4	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
20	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
21	1	L3	47 µH, ±10%, Unshielded, Wirewound Inductor, 1.56A, 140 mΩ Max, Radial	RLB0914-470KL	Bourns
22	1	Q1	MOSFET, N-CH, 100 V, 48 A (Tc), 113.5W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
23	1	R1	RES, 3.9 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ395V	Panasonic
24	2	R2, R4	RES, 1 MΩ, 5%, 1/8 W, Carbon Film	299-1M-RC	Xicon
25	1	R3	RES, 1.8 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ185V	Panasonic
26	1	R5	RES, 1.0 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105V	Panasonic
27	1	R6	RES, 3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ302V	Panasonic
28	2	R7, R8	RES, 47 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ470V	Panasonic
29	2	R9, R11	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
30	1	R10	RES, 390 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ394V	Panasonic
31	1	R12	RES, 10 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ100V	Panasonic
32	1	R13	RES, 0 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEY0R00V	Panasonic
33	1	R14	RES, 169 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1693V	Panasonic
34	1	R15	RES, 11.5 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1152V	Panasonic
35	1	R16	RES, 0.009 Ω, ±1%, 0.5 W, 0805, Current Sense, Moisture Resistant, Metal Element	CRF0805-FZ-R009ELF	Bourns
36	1	RV1	275 VAC, 23 J, 7 mm, RADIAL	V275LA4P	Littlefuse
37	1	T1	Bobbin, EQ25, 6 pins, 6pri, 0sec	POT-2501	Shenzhen xin yu jia
38	1	U1	MinE-CAP	MIN1072M	Power Integrations
39	1	U2	InnoSwitch-3EP, InSOP24D	INN3679C-H606	Power Integrations
40	1	VR1	DIODE ZENER 18 V 500 mW SOD123	MMSZ5248B-7-F	Diodes, Inc.

Miscellaneous

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	D, VO	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
2	3	GND, L, S	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
3	2	N, VBOT	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
4	1	V	Test Point, BLU, THRU-HOLE MOUNT	5127	Keystone
5	1	VTOP	Test Point, YEL, THRU-HOLE MOUNT	5014	Keystone
6	1	JP1	Wire Jumper, Non-Insulated, #18 AWG, 1.0 in	296 SV001	Alpha
7	1	JP2	Wire Jumper, Non-insulated, #28 AWG, 0.4 in	299/2 SV001	Digi-Key

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7 Transformer Specification

7.1 *Electrical Diagram*

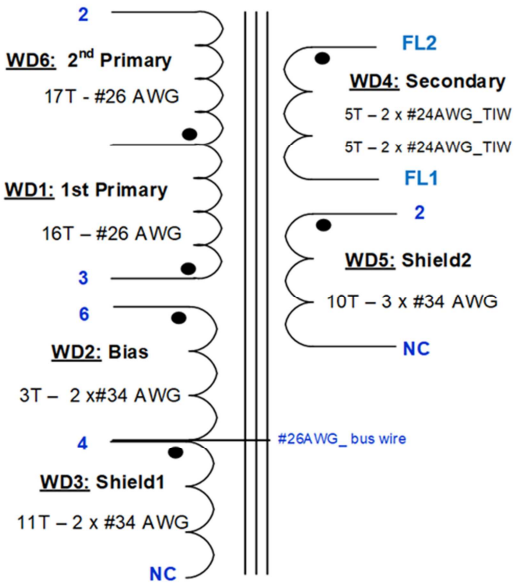

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 2 and 3, with all other windings open.	505 µH ±5%
Resonant Frequency	Between pin 2 and 3, other windings open.	1,000 kHz (Min.)
Primary Leakage Inductance	Between pin 2 and 3, with FL1-FL2 and pin 6-4 shorted.	4.5 µH (Max).

7.3 *Material List*

Item	Description
[1]	Core: EQ25, Ferroxcube: 3C95.
[2]	Bobbin: EQ25-Vert-6pins (6/0); PI#: 25-01136-00.
[3]	Magnet Wire: #26 AWG, Double Coated.
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	Magnet Wire: #24 AWG, Triple Insulated Wire.
[6]	Bus Wire: #26AWG, Alpha wire, tinned copper.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 7.5mm Width.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 33 mm x 58 mm.
[9]	Varnish: Dolph BC-359.
[10]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 15 mm x 88 mm.

7.4 *Transformer Build Diagram*

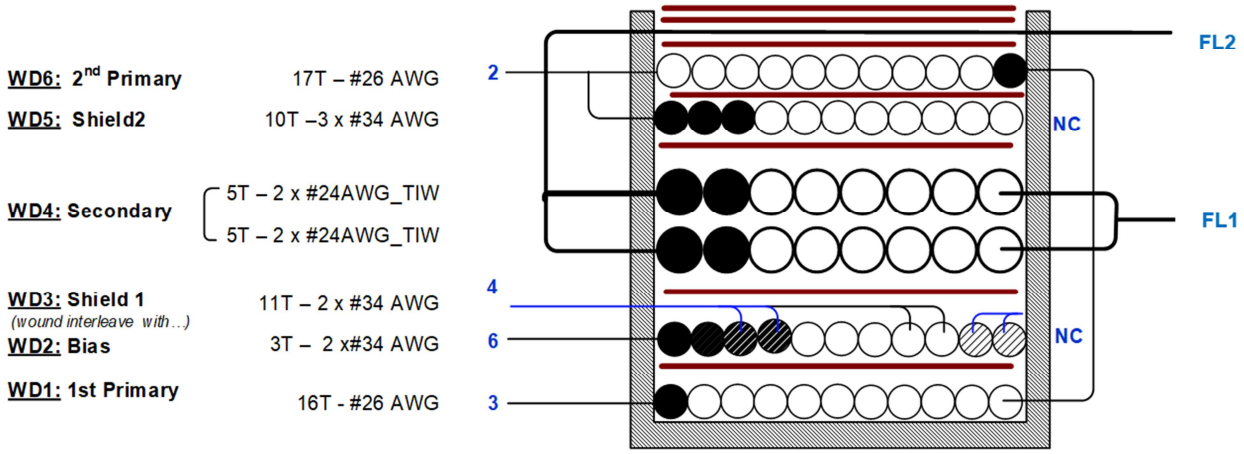

Figure 7 – Transformer Build Diagram.

7.5 *Transformer Instructions*

Winding Preparation	Make slots with 2.0mm width on both flanges of secondary side of bobbin Item [2]. Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 1st Primary	Start at pin 3, wind 16 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn, leave the wire floating and enough length for WD6-2nd Primary.
Insulation	1 layer of tape Item [7].
WD2: Bias & WD3: Shield1	Use 2 wires Item [4] start at pin 6 for bias winding, also use 2 wires same Item [4] start at pin 4 for Shield1 winding. Wind all 4 wires in parallel, at the 3rd turn, place 1 piece of tape to hold the wires, and bring first 2 wires for bias winding to the left to terminate at pin 4. Continue winding other 2 wires with 8 turns, at the last turn cut short to leave as No-Connect.
Insulation	1 layer of tape Item [7].
WD4 Secondary	Start at left slot of secondary side, use 2 wires Item [5], leaving ~40.0 mm, and mark as FL2.Wind 5 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 30.0mm and mark FL1. Repeat the same winding above on top previous winding, also mark start and finish ends as FL2 and FL1.
Insulation	1 layer of tape Item [7].
WD5 Shield2	Start at pin 2, wind 10 tri-filar turns of wire Item [4], from left to right. At the last turn, cut short to leave as No-Connect.
Insulation	1 layer of tape Item [7].
WD6 2nd Primary	Use floating wire from WD1-1st Primary, wind 17 turns from right to left and finish at pin 2.
Insulation	1 layer of tape Item [7].
Finish	Bring 4 wires marked as FL2 to the right and secure with 2 layers of tape Item [7]. Gap core halves to get 505uH. Solder pin 4 with bus-wire Item [6] then lean along core halves and secure with 1 layer tape Item [10]. Varnish with Item [9]. Place 2 layers of tape Item [8] at the bottom then wrap up to the body of transformer, and tape around 1layer of tape Item [7].

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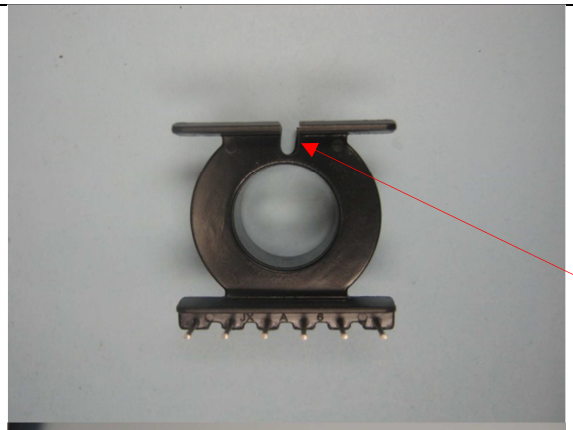
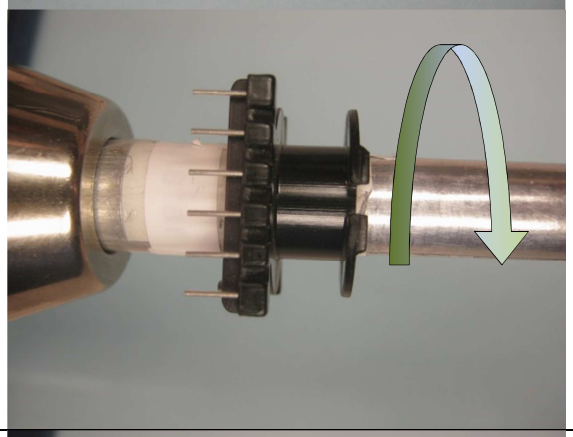
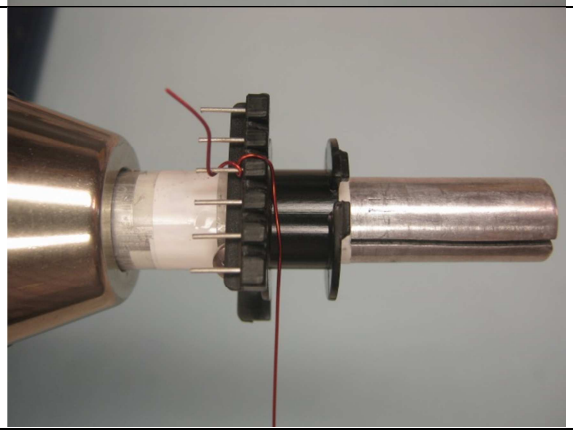
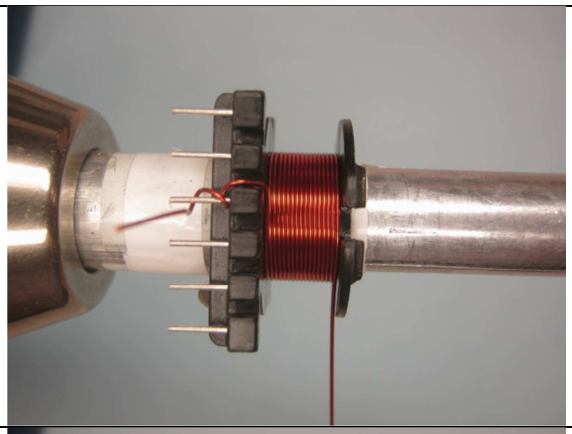
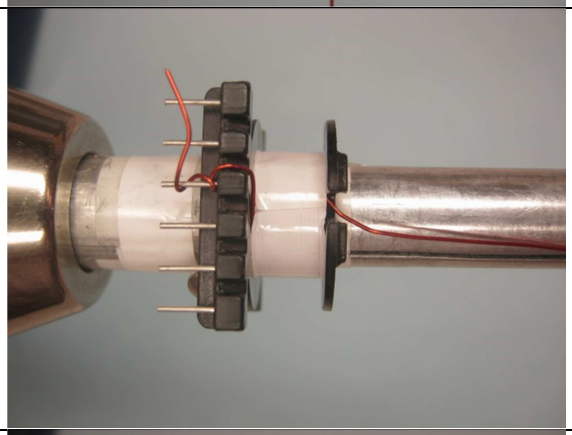
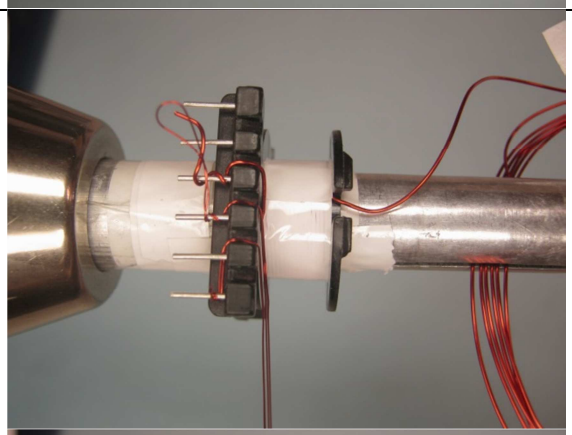
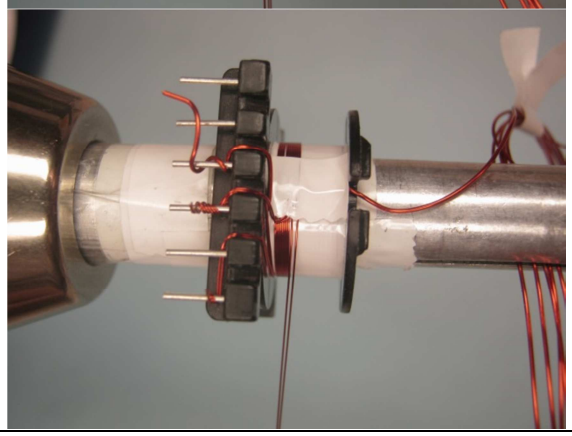
7.6 *Transformer Winding Illustrations*

Winding Preparation	 	Make slots with 2.0 mm width on both flanges of secondary side of bobbin Item [2]. Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction. (*see beside picture)*
WD1 **1st Primary**		Start at pin 3, wind 16 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn, leave the wire floating and enough length for WD6-2nd Primary.

		
Insulation		1 layer of tape Item [7].
WD2: Bias **&** **WD3: Shield1**	 	Use 2 wires Item [4] start at pin 6 for bias winding, also use 2 wires same Item [4] start at pin 4 for Shield1 winding. Wind all 4 wires in parallel, at the 3rd turn, place 1 piece of tape to hold the wires, and bring first 2 wires for bias winding to the left to terminate at pin 4. Continue winding other 2 wires with 8 turns, at the last turn cut short to leave as No-Connect.

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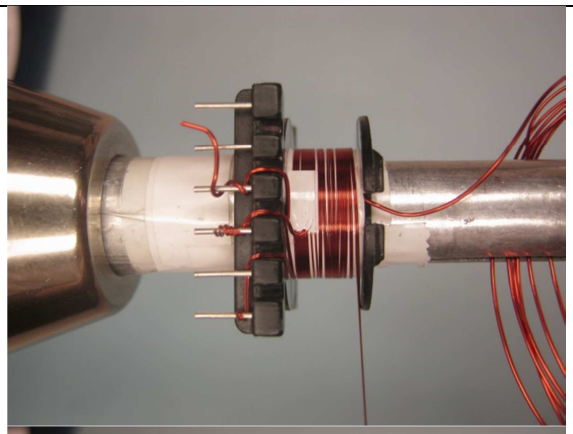
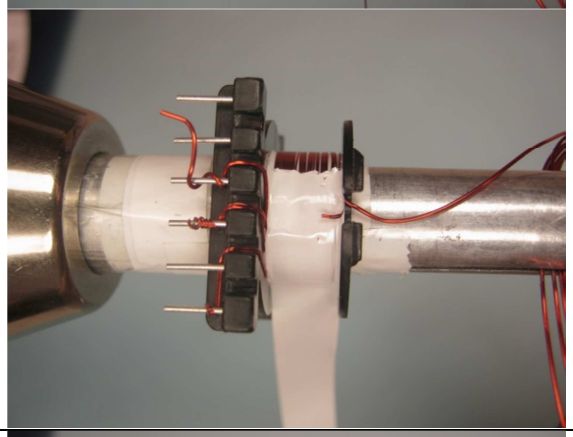
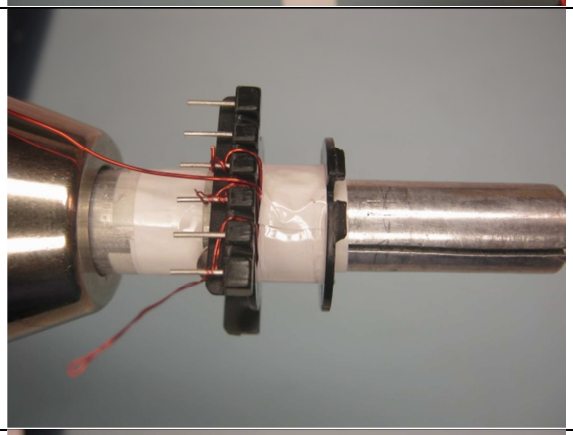
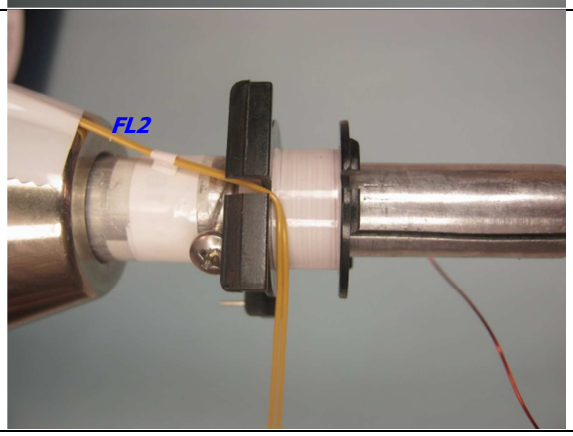
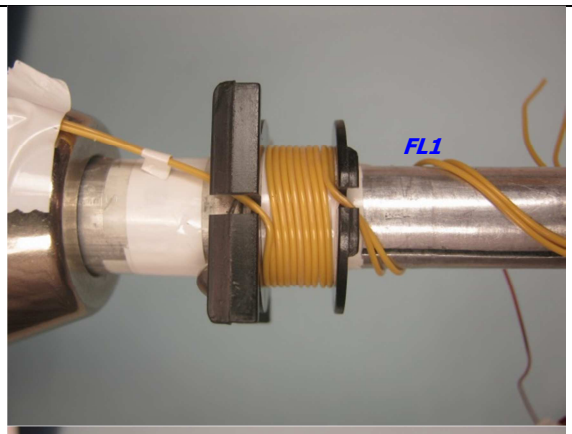
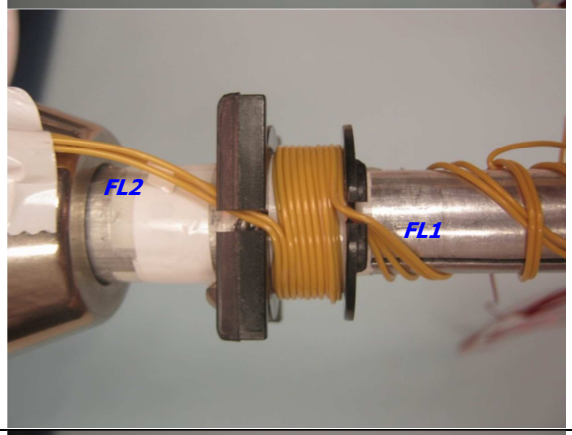
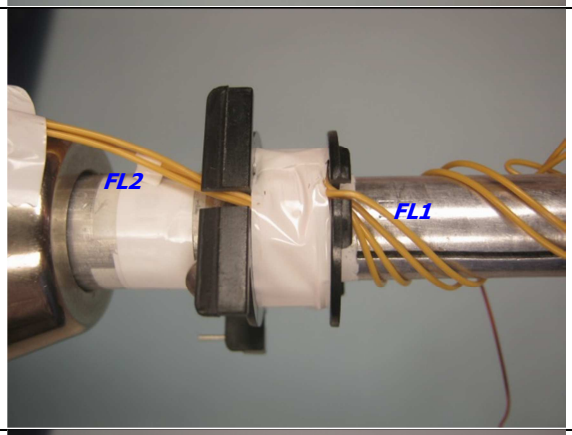
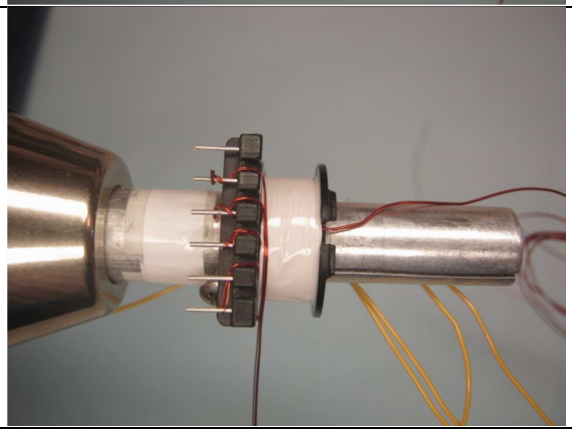
	 	
Insulation		1 layer of tape Item [7].
WD4 Secondary		Start at left slot of secondary side, use 2 wires Item [5], leaving ~ 40.0mm, and mark as FL2.Wind 5 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 30.0mm and mark FL1. Repeat the same winding above on top previous winding, also mark start and finish ends as FL2 and

	 	FL1.
Insulation		1 layer of tape Item [7].
WD5 **Shield2**		Start at pin 2, wind 10 tri-filar turns of wire Item [4], from left to right. At the last turn, cut short to leave as No-Connect.

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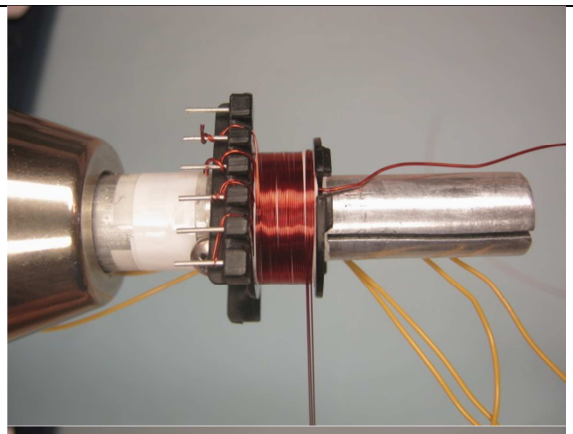
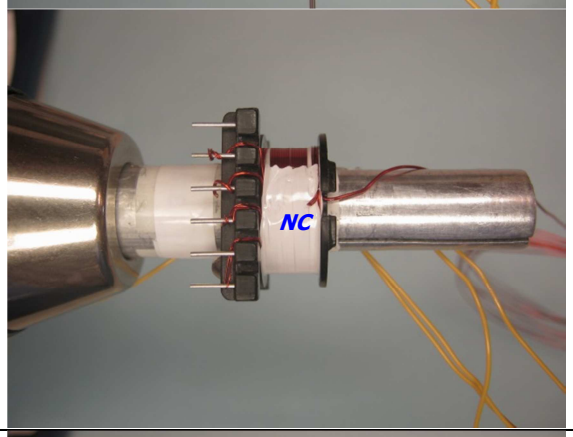
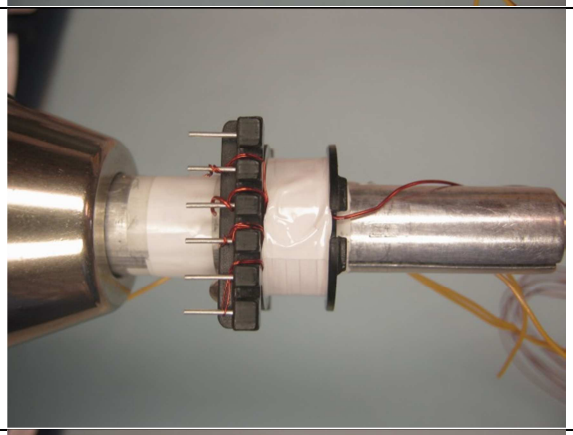
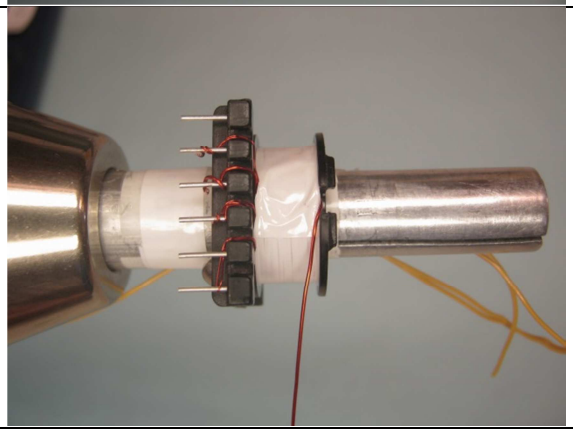
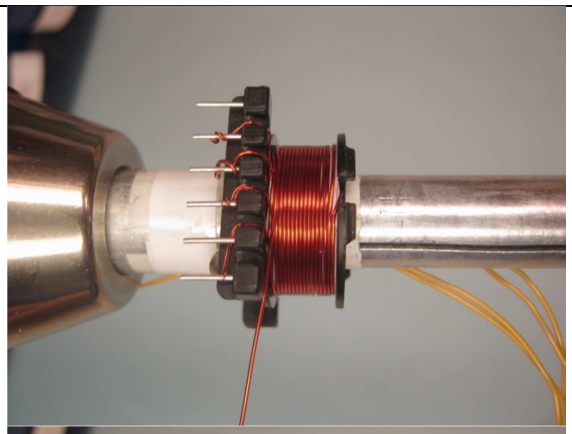
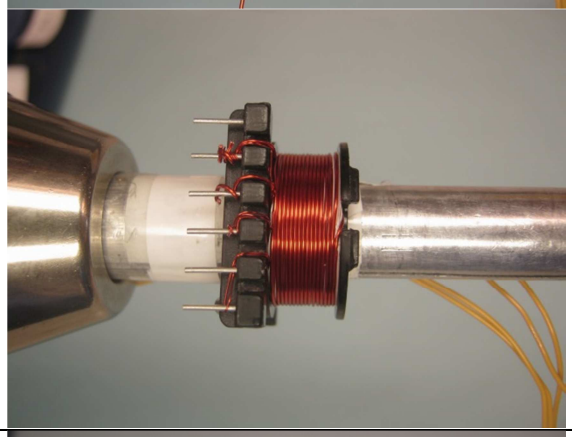
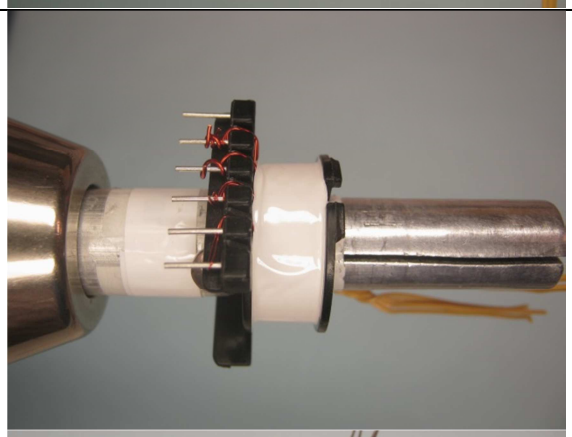
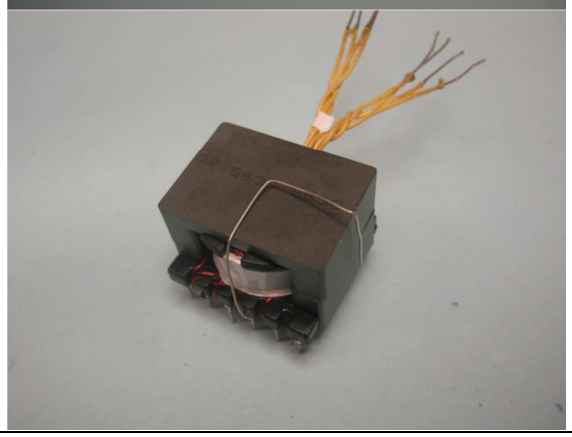
	 	
Insulation		1 layer of tape Item [7].
WD6 **2nd Primary**		Use floating wire from WD1-1st Primary, wind 17 turns from right to left and finish at pin 2.

	 	
Finish	 	Bring 4 wires marked as FL2 to the right and secure with 2 layers of tape Item [7]. Gap core halves to get 505uH. Solder pin 4 with bus-wire Item [6] then lean along core halves and secure with 1 layer tape Item [10]. Varnish with Item [9]. Place 2 layers of tape Item [8] at the bottom then wrap up to the body of transformer, and tape around 1 layer of tape Item [7]. (*See pictures beside*).

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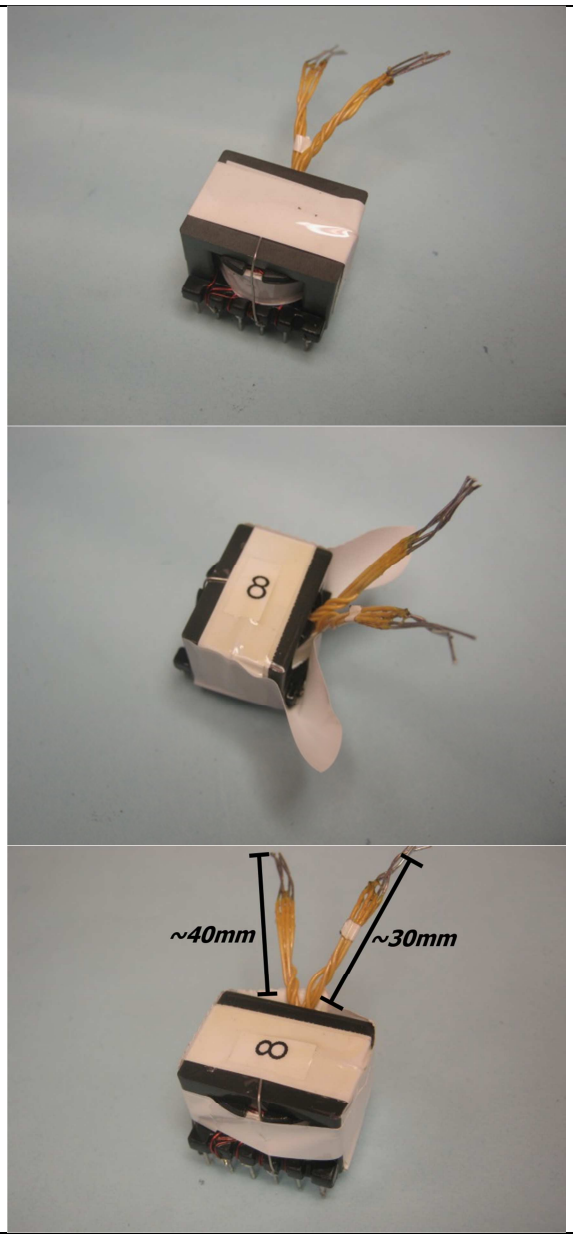
8
~40mm
~30mm
8

8 Design Spreadsheet

1	ACDC_Flyback_081518; Rev.0.1; Copyright Power Integrations 2018	INPUT	INFO	OUTPUT	UNITS	Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VAC_MIN	90		90	V	Minimum AC line voltage
4	VAC_MAX			265	V	Maximum AC input voltage
5	VAC_RANGE			UNIVERSAL		AC line voltage range
6	FLINE			60	Hz	AC line voltage frequency
7	CAP_INPUT	100.0		100.0	uF	Input capacitance
9	**SETPOINT 1**					
10	VOUT1	20.00		20.00	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	3.250		3.250	A	Output current 1
12	POUT1			65.00	W	Output power 1
13	EFFICIENCY1	0.92		0.92		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
73	CDC_SCALING_SETPOINT	1		1		Select the setpoint number for the voltage used for cable drop compensation (typically the 5V output)
77	**PRIMARY CONTROLLER SELECTION**					
78	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
79	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
80	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
81	DEVICE_GENERIC	AUTO		INN3679C		Device selection
82	DEVICE_CODE			INN3679C		Device code
83	PDEVICE_MAX			65	W	Device maximum power capability
84	RDSON_25DEG			0.34	Ω	Primary MOSFET on-time resistance at 25°C
85	RDSON_100DEG			0.53	Ω	Primary MOSFET on-time resistance at 100°C
86	ILIMIT_MIN			1.981	A	Primary MOSFET minimum current limit
87	ILIMIT_TYP			2.130	A	Primary MOSFET typical current limit
88	ILIMIT_MAX			2.279	A	Primary MOSFET maximum current limit
89	VDRAIN_ON_MOSFET			0.42	V	Primary MOSFET on-time voltage drop
90	VDRAIN_OFF_MOSFET			573.31	V	Peak drain voltage on the primary MOSFET during turn-off
94	**WORST CASE ELECTRICAL PARAMETERS**					
95	FSWITCHING_MAX	84500		84500	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
96	VOR	130.0		130.0	V	Voltage reflected to the primary winding (corresponding to setpoint 1) when the primary MOSFET turns off
97	VMIN			86.84	V	Valley of the rectified minimum input AC voltage at full load
98	KP			0.646		Measure of continuous/discontinuous mode of operation
99	MODE_OPERATION			CCM		Mode of operation
100	DUTYCYCLE			0.601		Primary MOSFET duty cycle
101	TIME_ON			11.66	us	Primary MOSFET on-time
102	TIME_OFF			4.73	us	Primary MOSFET off-time
103	LPRIMARY_MIN			479.7	uH	Minimum primary magnetizing inductance
104	LPRIMARY_TYP			504.9	uH	Typical primary magnetizing inductance
105	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
106	LPRIMARY_MAX			530.2	uH	Maximum primary magnetizing inductance
108	**PRIMARY CURRENT**					
109	IAVG_PRIMARY			0.785	A	Primary MOSFET average current
110	IPEAK_PRIMARY			2.156	A	Primary MOSFET peak current

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111	IPEDESTAL_PRIMARY			0.683	A	Primary MOSFET current pedestal
112	IRIPPLE_PRIMARY			1.698	A	Primary MOSFET ripple current
113	IRMS_PRIMARY			1.082	A	Primary MOSFET RMS current
115	**SECONDARY CURRENT**					
116	IPEAK_SECONDARY			14.227	A	Secondary MOSFET peak current
117	IPEDESTAL_SECONDARY			4.509	A	Secondary MOSFET pedestal current
118	IRMS_SECONDARY			5.820	A	Secondary MOSFET RMS current
119	IRIPPLE_CAP_OUT			4.828	A	Output capacitor ripple current
123	**TRANSFORMER CONSTRUCTION PARAMETERS**					
124	**CORE SELECTION**					
125	CORE	CUSTOM		CUSTOM		Core selection
126	CORE NAME	EQ25		EQ25		Core code
127	AE	100.0		100.0	mm^2	Core cross sectional area
128	LE	41.4		41.4	mm	Core magnetic path length
129	AL	5700		5700	nH	Ungapped core effective inductance per turns squared
130	VE	4145		4145	mm^3	Core volume
131	BOBBIN NAME	EQ25		EQ25		Bobbin name
132	AW	52.0		52.0	mm^2	Bobbin window area
133	BW	7.60		7.60	mm	Bobbin width
134	MARGIN			0.0	mm	Bobbin safety margin
136	**PRIMARY WINDING**					
137	NPRIMARY			33		Primary winding number of turns
138	BPEAK			3748	Gauss	Peak flux density
139	BMAX			3423	Gauss	Maximum flux density
140	BAC			1324	Gauss	AC flux density (0.5 x Peak to Peak)
141	ALG			464	nH	Typical gapped core effective inductance per turns squared
142	LG			0.249	mm	Core gap length
143	LAYERS_PRIMARY			2		Primary winding number of layers
144	AWG_PRIMARY	26		26		Primary wire gauge
145	OD_PRIMARY_INSULATED			0.465	mm	Primary wire insulated outer diameter
146	OD_PRIMARY_BARE			0.405	mm	Primary wire bare outer diameter
147	CMA_PRIMARY			234.9	Cmils/A	Primary winding wire CMA
149	**SECONDARY WINDING**					
150	NSECONDARY	5		5		Secondary winding number of turns
151	AWG_SECONDARY			19		Secondary wire gauge
152	OD_SECONDARY_INSULATED			1.217	mm	Secondary wire insulated outer diameter
153	OD_SECONDARY_BARE			0.912	mm	Secondary wire bare outer diameter
154	CMA_SECONDARY			221.3	Cmils/A	Secondary winding wire CMA
156	**BIAS WINDING**					
157	NBIAS			3		Bias winding number of turns
161	**PRIMARY COMPONENTS SELECTION**					
162	**LINE UNDERVOLTAGE**					
163	BROWN-IN REQURED			72.00	V	Required line brown-in threshold
164	RLS			3.56	MΩ	Connect two 1.78 MOhm resistors to the V-pin for the required UV/OV threshold
165	BROWN-IN ACTUAL			71.40	V	Actual brown-in threshold using standard resistors
166	BROWN-OUT ACTUAL			64.58	V	Actual brown-out threshold using standard resistors
168	**LINE OVERVOLTAGE**					
169	OVERVOLTAGE_LINE			297.50	V	Actual AC RMS line over-voltage threshold
170						
171	BIAS WINDING					
172	VBIAS			9.00	V	Rectified bias voltage at the lowest output setpoint

173	VF_BIAS			0.70	V	Bias winding diode forward drop
174	VREVERSE_BIASDIODE			42.94	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
175	CBIAS			22	uF	Bias winding rectification capacitor
176	CBPP			4.70	uF	BPP pin capacitor
180	**SECONDARY COMPONENTS SELECTION**					
181	**RECTIFIER**					
182	VDRAIN_OFF_SRFET			76.56	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
183	SRFET	AUTO		AO4294		Secondary rectifier (Logic MOSFET)
184	VBREAKDOWN_SRFET			100	V	Secondary rectifier breakdown voltage
185	RDSON_SRFET			15.5	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
187	**FEEDBACK COMPONENTS**					
188	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
189	RFB_LOWER			6.81	kΩ	Lower feedback resistor required to obtain the output for cable drop compensation
190	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
194	**SETPOINTS ANALYSIS**					
195	**TOLERANCE CORNER**					
196	USER_VAC	115		115	V	Input AC RMS voltage corner to be evaluated
197	USER_ILIMIT	TYP		2.130	A	Current limit corner to be evaluated
198	USER_LPRIMARY	TYP		504.9	uH	Primary inductance corner to be evaluated
200	**SETPOINT SELECTION**					
201	SETPOINT	1		1		Select the setpoint which needs to be evaluated
202	FSWITCHING			65628.5	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
203	VOR			130.0	V	Voltage reflected to the primary winding when the primary MOSFET turns off
204	VMIN			131.28	V	Valley of the minimum input AC voltage
205	KP			0.973		Measure of continuous/discontinuous mode of operation
206	MODE_OPERATION			CCM		Mode of operation
207	DUTYCYCLE			0.498		Primary MOSFET duty cycle
208	TIME_ON			7.71	us	Primary MOSFET on-time
209	TIME_OFF			7.65	us	Primary MOSFET off-time
211	**PRIMARY CURRENT**					
212	IAVG_PRIMARY			0.518	A	Primary MOSFET average current
213	IPEAK_PRIMARY			2.024	A	Primary MOSFET peak current
214	IPEDESTAL_PRIMARY			0.055	A	Primary MOSFET current pedestal
215	IRIPPLE_PRIMARY			1.969	A	Primary MOSFET ripple current
216	IRMS_PRIMARY			0.836	A	Primary MOSFET RMS current
218	**SECONDARY CURRENT**					
219	IPEAK_SECONDARY			13.358	A	Secondary MOSFET peak current
220	IPEDESTAL_SECONDARY			0.363	A	Secondary MOSFET pedestal current
221	IRMS_SECONDARY			5.540	A	Secondary MOSFET RMS current
222	IRIPPLE_CAP_OUT			4.486	A	Output capacitor ripple current
224	**MAGNETIC FLUX DENSITY**					
225	BPEAK			3336	Gauss	Peak flux density
226	BMAX			3097	Gauss	Maximum flux density
227	BAC			1506	Gauss	AC flux density (0.5 x Peak to Peak)

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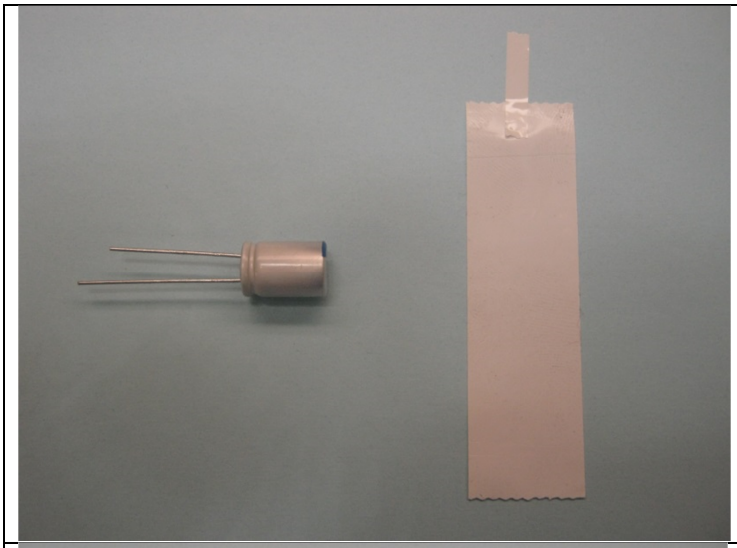
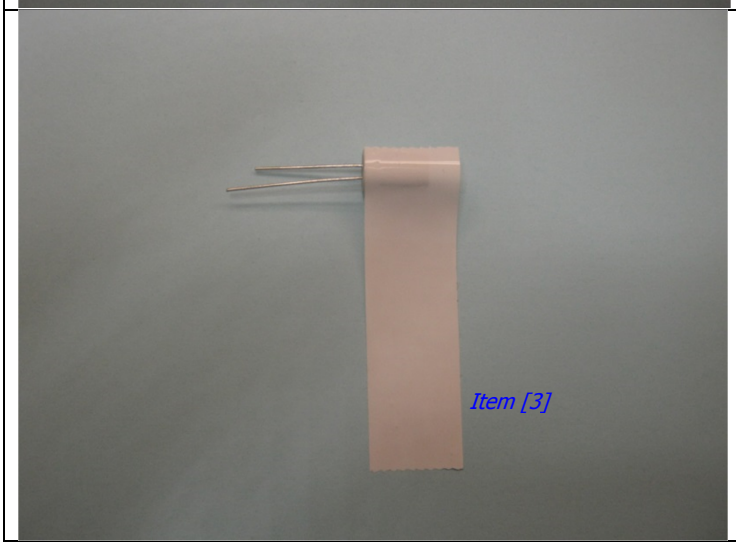
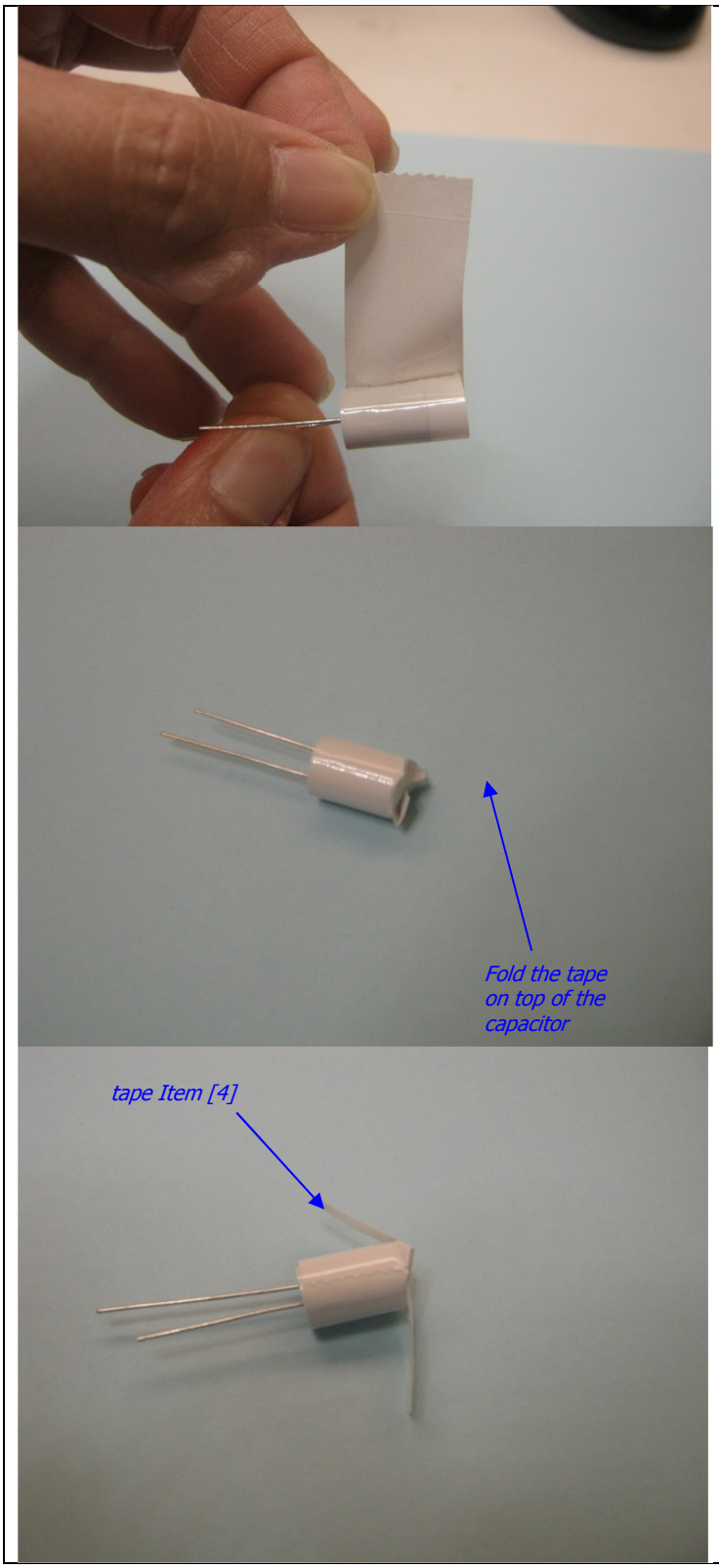
9 PCB Assembly Instructions

9.1 *Materials*

Item	Description
[1]	Capacitor C12 on DER-726 Schematic.
[2]	Capacitor C14 on DER-726 Schematic.
[3]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 16.4 mm Wide, 25 mm Long.
[4]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 5.0 mm Wide, 15 mm Long.
[5]	Fill up the vias by soldering lead.

9.2 *Output Capacitor Assembly Instructions*

	
	Wrap C12 and C14 with tape Item [3] to insulate the capacitor form transformer core.



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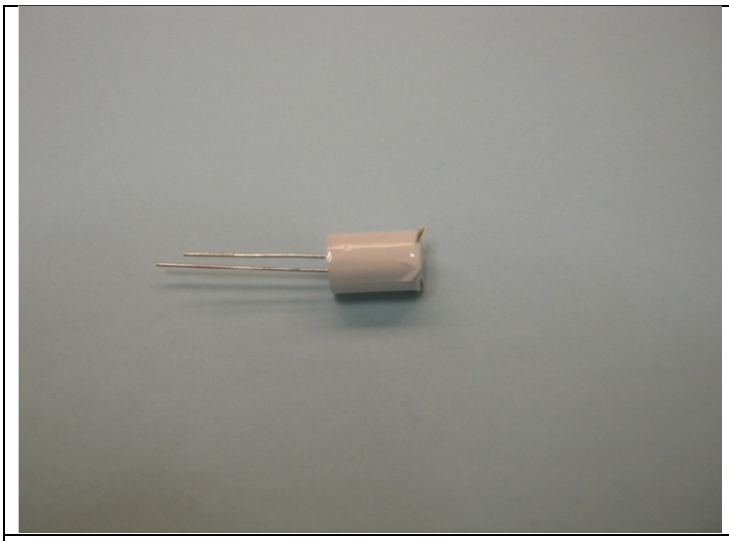
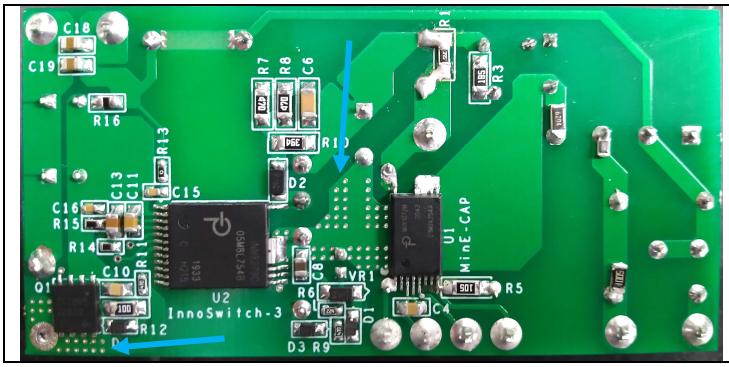
	
	Finish assembly.

Note: Cut all the excess capacitor leads to <0.5 mm on the bottom side of the board after completing the assembly.

9.3 *Solder fill Instructions*

	Fill in vias by soldering the lead for better heat sinking.

10 Performance Data

10.1 *Efficiency*

10.1.1 Average Efficiency

10.1.1.1 90 VAC / 60 Hz.

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	90	1338.1	69.09	19.589	3249.2	63.65	92.126
75%	90	1044.6	51.49	19.657	2436.5	47.9	93.028
50%	90	753.2	34.44	19.751	1624.2	32.08	93.148
25%	90	436.8	17.25	19.777	811.5	16.049	93.038
						Average	**92.835**

10.1.1.2 115 VAC / 60 Hz.

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} m(A_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	115	1255.7	68.66	19.624	3249.2	63.76	92.863
75%	115	1015.6	51.51	19.702	2436.6	48.01	93.205
50%	115	748.2	34.39	19.758	1624.2	32.09	93.312
25%	115	300.2	17.2	19.781	811.5	16.053	93.331
						Average	**93.17775**

10.1.1.3 230 VAC / 50 Hz.

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	230	572.1	67.73	19.686	3249.1	63.96	94.434
75%	230	456.9	51.01	19.746	2436.5	48.11	94.315
50%	230	334.3	34.14	19.776	1624.2	32.12	94.083
25%	230	198.29	17.24	19.797	811.6	16.067	93.196
						Average	**94.007**

10.1.1.4 265 VAC / 50 Hz.

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	265	527.7	67.83	19.704	3249.1	64.02	94.383
75%	265	423.2	51.08	19.749	2436.6	48.12	94.205
50%	265	311.4	34.21	19.778	1624.2	32.12	93.891
25%	265	186.14	17.31	19.8	811.6	16.069	92.831
						Average	**93.8275**

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10.1.2 Full Load Efficiency vs. Line

Test Condition: Soak for 5 minutes for each line.

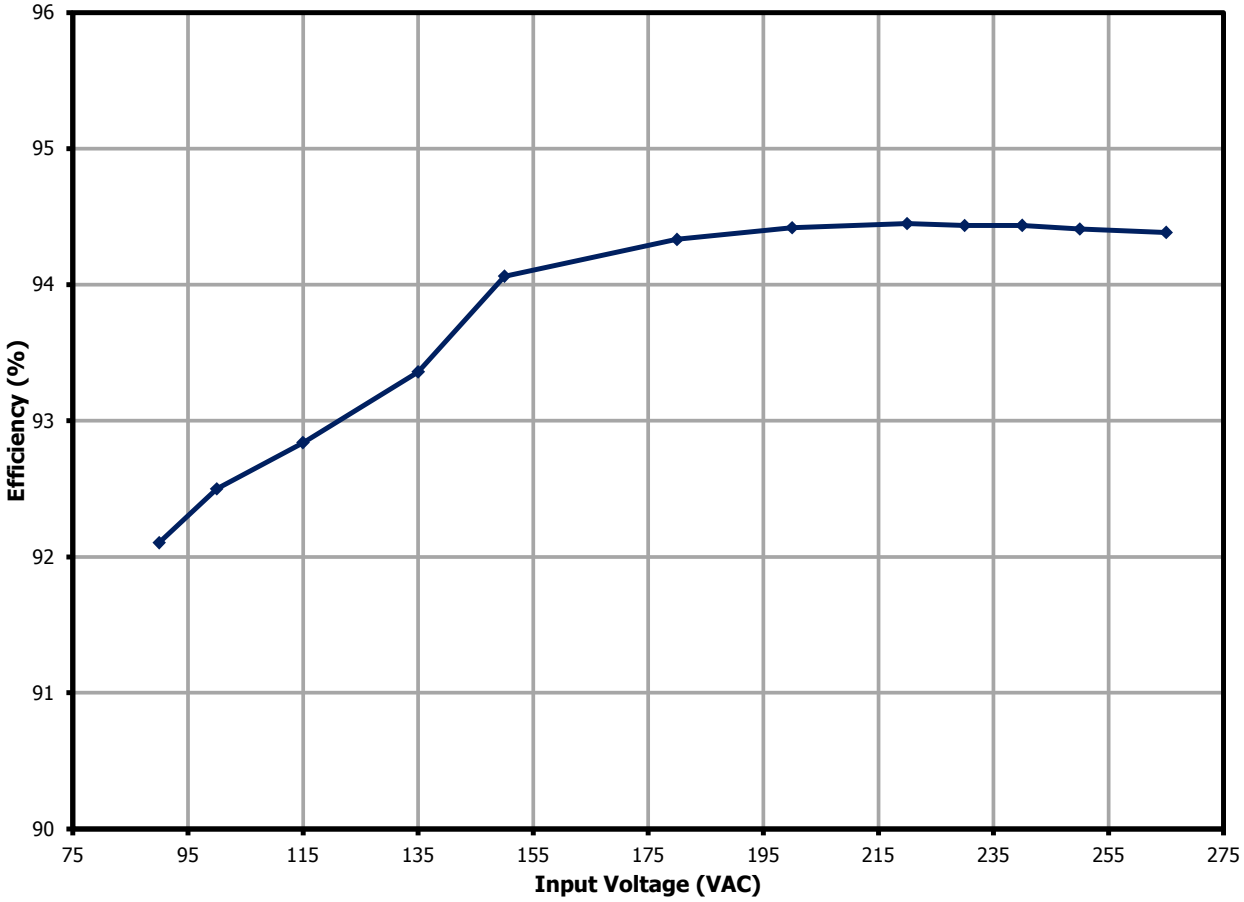

Figure 8 – Full Load Efficiency vs. Line.

10.1.3 Efficiency vs. Load

Test Condition: Soak for 5 minutes each line, and 30 seconds for each load.

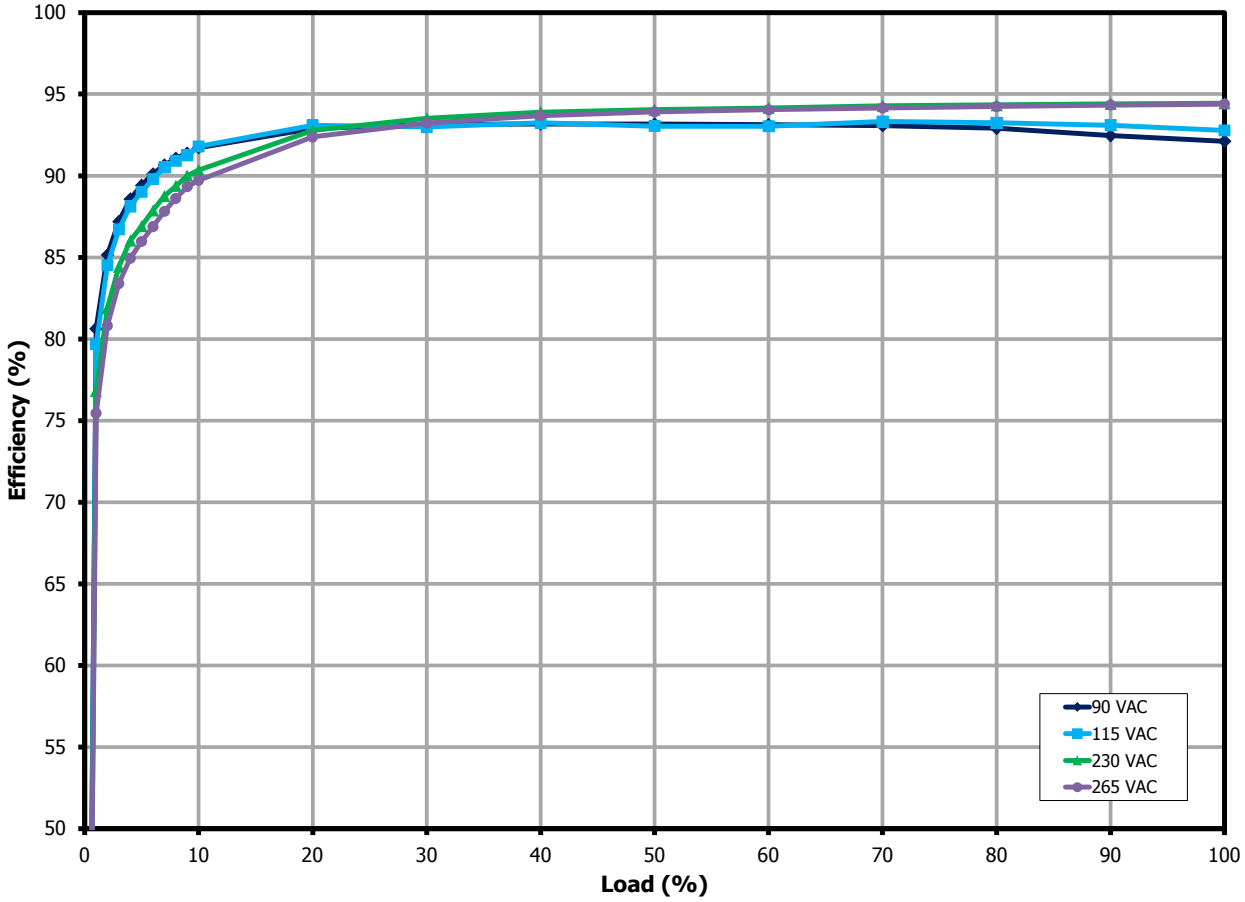

Figure 9 – Efficiency vs. Percentage Load.

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10.2 *Available Standby Output Power*

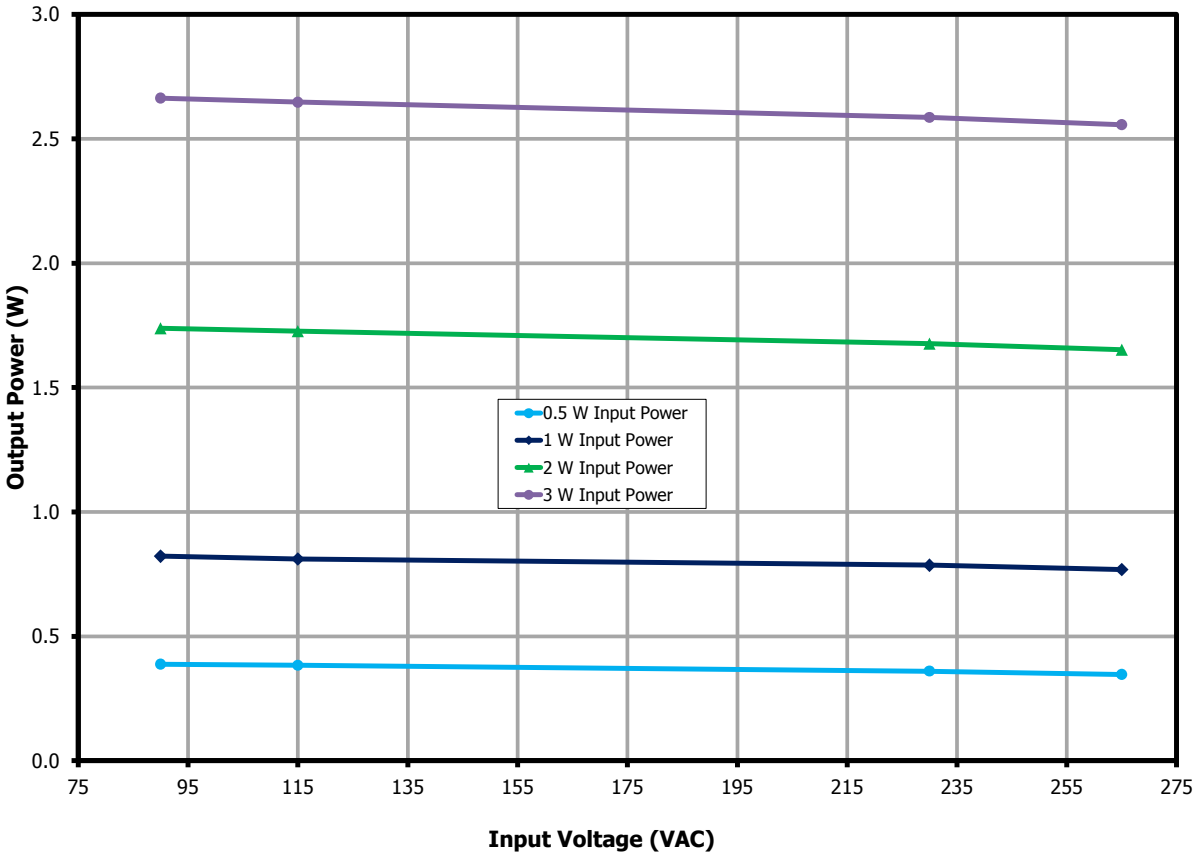

Figure 10 – Available Standby Output Power for 0.5 W, 1 W, 2 W and 3 W Input Power.

10.3 ***No-Load Input Power***

Test Condition: Soak for 5 minutes each line and 2-minute integration time.

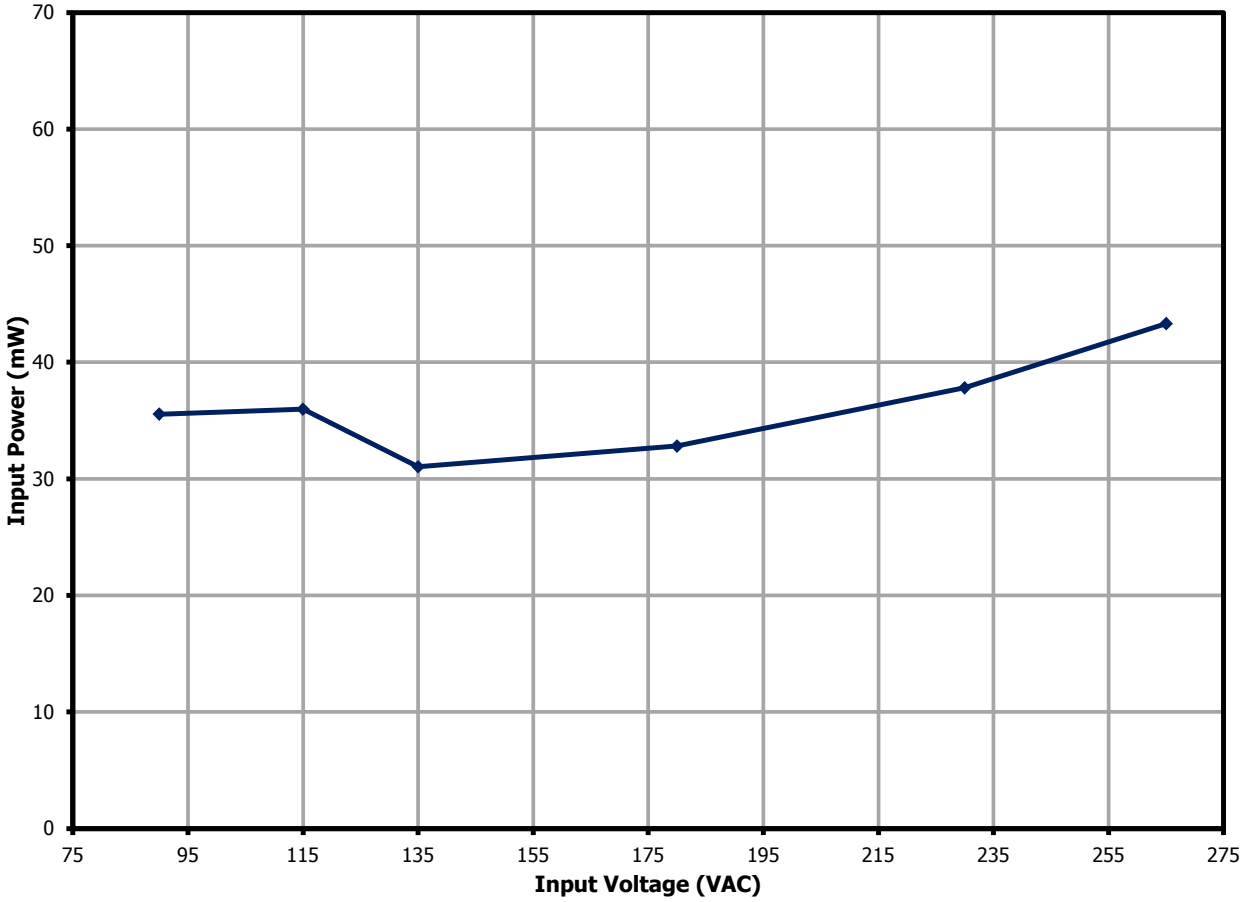

Figure 11 – No-Load Input Power vs. Line at Room Temperature.

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10.4 ***Line Regulation***

Test Condition: Soak for 5 minutes for each line.

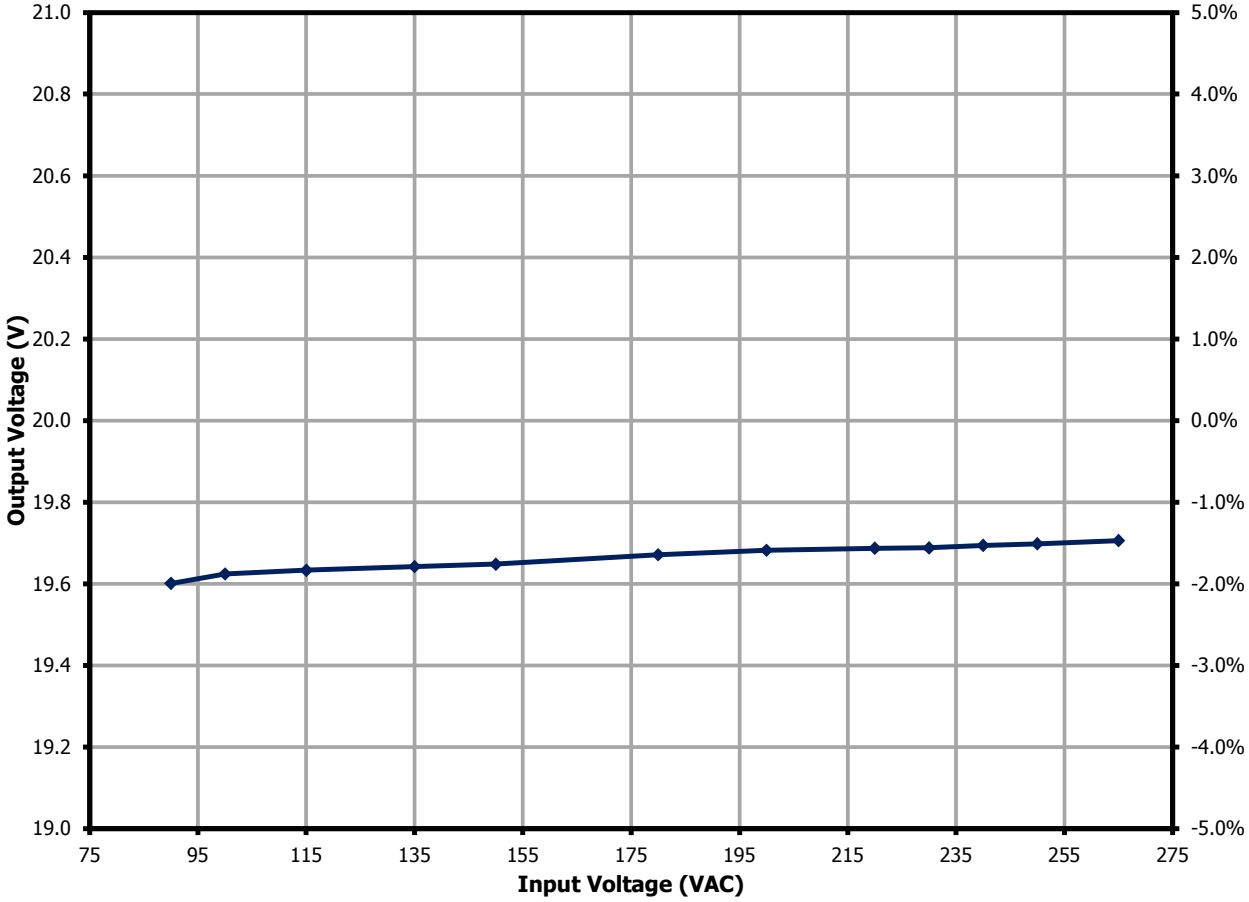

Figure 12 – Output Voltage vs. Line Voltage.

10.5 ***Load Regulation***

Test Condition: Soak for 5 minutes each line, and 30 seconds for each load.

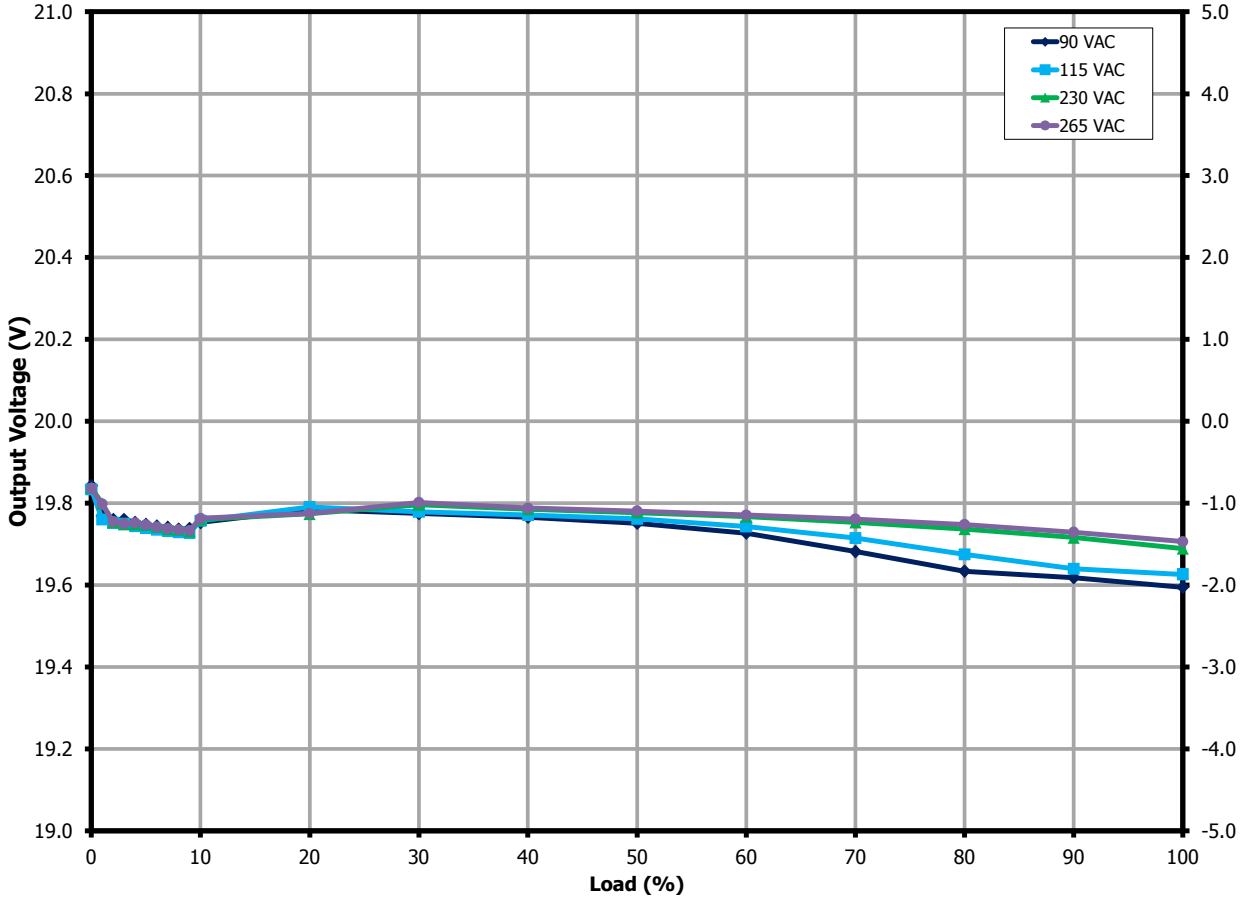

Figure 13 – Output Voltage vs. Percent Load.

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11 Waveforms

11.1 *Load Transient Response*

Test Condition: Frequency = 500 Hz., Duty cycle = 50 %, Slew Rate = 800 mA / µs

11.1.1 0% - 100% Load Change

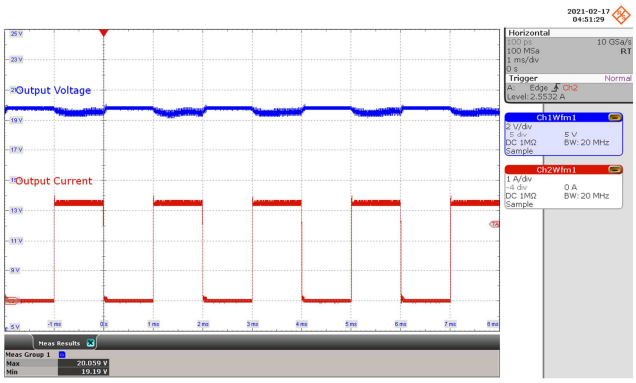

Figure 14 – 90 VAC 60 Hz.
CH1: Output Voltage, 2 V / div., 1 ms / div.
CH2: Output Current, 1 A / div., 1 ms / div.
V_{MAX}: 20.06 V, V_{MIN}: 19.19 V.

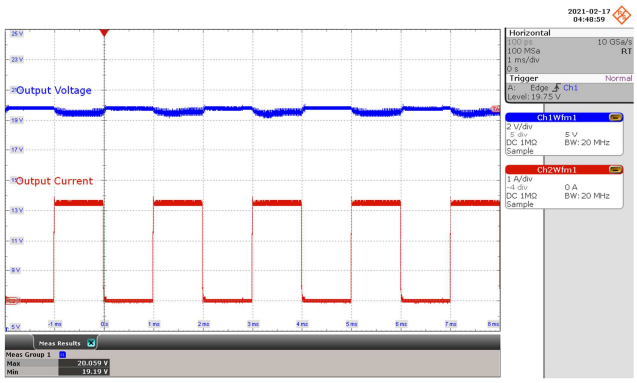

Figure 15 – 115 VAC 60 Hz.
CH1: Output Voltage, 2 V / div., 1 ms / div.
CH2: Output Current, 1 A / div., 1 ms / div.
V_{MAX}: 20.06 V, V_{MIN}: 19.19 V.

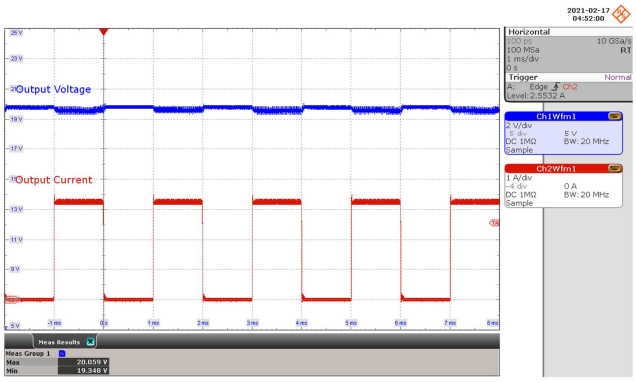

Figure 16 – 230 VAC 60 Hz.
CH1: Output Voltage, 2 V / div., 1 ms / div.
CH2: Output Current, 1 A / div., 1 ms / div.
V_{MAX}: 20.06 V, V_{MIN}: 19.35 V.

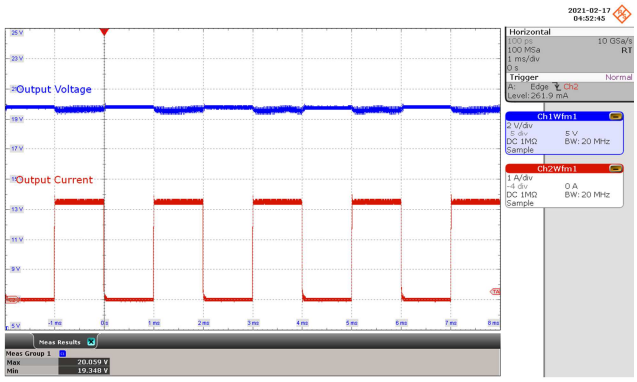

Figure 17 – 265 VAC 60 Hz.
CH1: Output Voltage, 2 V / div., 1 ms / div.
CH2: Output Current, 1 A / div., 1 ms / div.
V_{MAX}: 20.06 V, V_{MIN}: 19.35 V.

11.1.2 50% - 100% Load Change

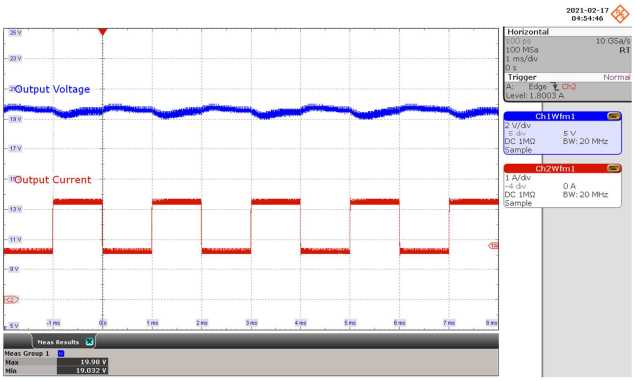

Figure 18 – 90 VAC 60 Hz.
CH1: Output Voltage, 2 V / div., 1 ms / div.
CH2: Output Current, 1 A / div., 1 ms / div.
V_{MAX}: 19.98 V, V_{MIN}: 19.03 V.

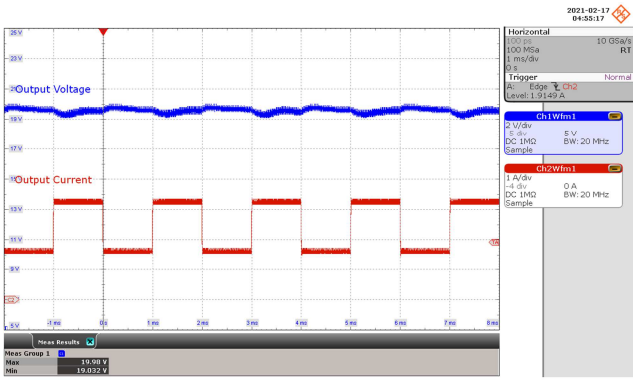

Figure 19 – 115 VAC 60 Hz.
CH1: Output Voltage, 2 V / div., 1 ms / div.
CH2: Output Current, 1 A / div., 1 ms / div.
V_{MAX}: 19.98 V, V_{MIN}: 19.03 V.

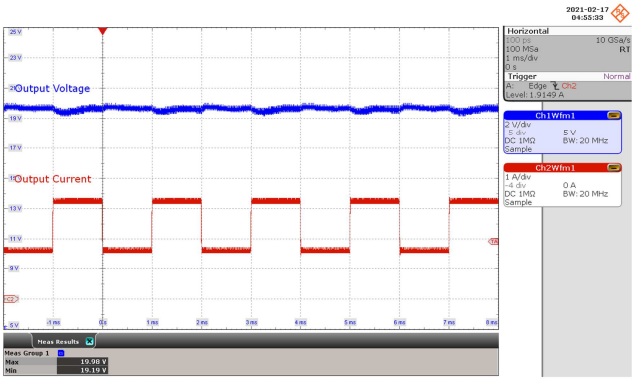

Figure 20 – 230 VAC 60 Hz.
CH1: Output Voltage, 2 V / div., 1 ms / div.
CH2: Output Current, 1 A / div., 1 ms / div.
V_{MAX}: 19.98 V, V_{MIN}: 19.19 V.

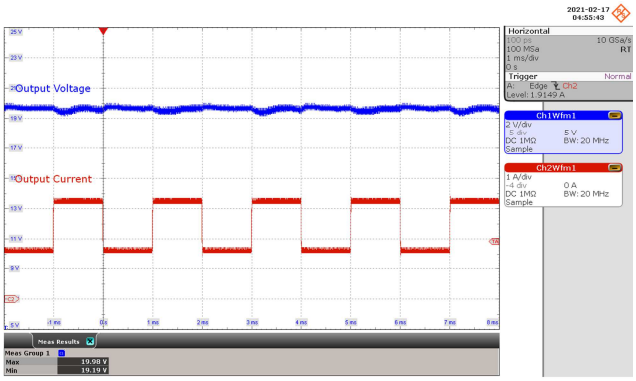

Figure 21 – 265 VAC 60 Hz.
CH1: Output Voltage, 2 V / div., 1 ms / div.
CH2: Output Current, 1 A / div., 1 ms / div.
V_{MAX}: 19.98 V, V_{MIN}: 19.19 V.

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11.2 *Output Voltage at Start-up*

11.2.1 CC Mode

11.2.1.1 100% Load

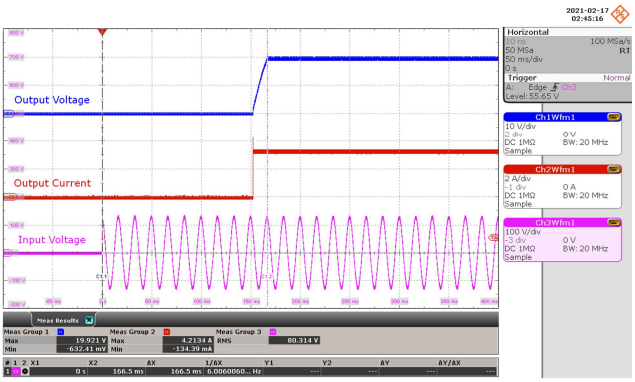

Figure 22 – 90 VAC 60 Hz.
CH1: Output Voltage, 10 V / div., 50 ms / div.
CH2: Output Current, 2 A / div., 50 ms / div.
CH3: Input Voltage, 100 V / div., 50 ms / div.
On-Time Delay = 166.5 ms.

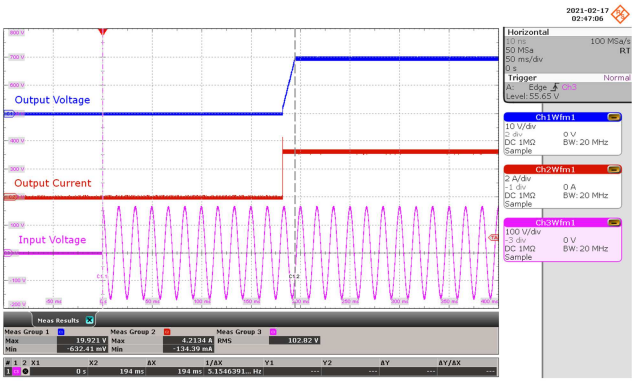

Figure 23 – 115 VAC 60 Hz.
CH1: Output Voltage, 10 V / div., 50 ms / div.
CH2: Output Current, 2 A / div., 50 ms / div.
CH3: Input Voltage, 100 V / div., 50 ms / div.
On-Time Delay = 194 ms.

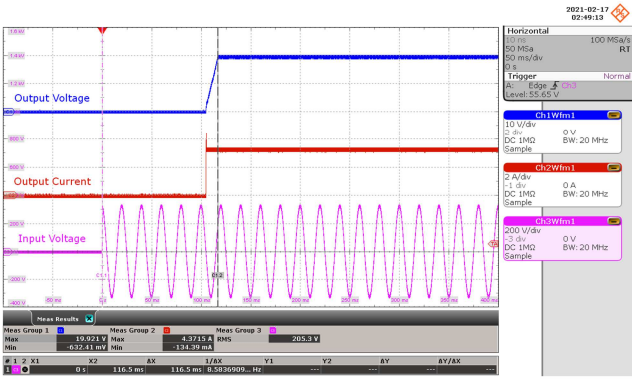

Figure 24 – 230 VAC 60 Hz.
CH1: Output Voltage, 10 V / div., 50 ms / div.
CH2: Output Current, 2 A / div., 50 ms / div.
CH3: Input Voltage, 200 V / div., 50 ms / div.
On-Time Delay = 116.5 ms.

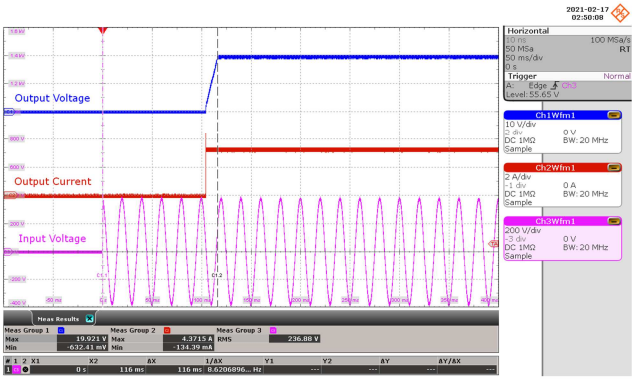

Figure 25 – 265 VAC 60 Hz.
CH1: Output Voltage, 10 V / div., 50 ms / div.
CH2: Output Current, 2 A / div., 50 ms / div.
CH3: Input Voltage, 200 V / div., 50 ms / div.
On-Time Delay = 116 ms.

11.2.1.2 0% Load

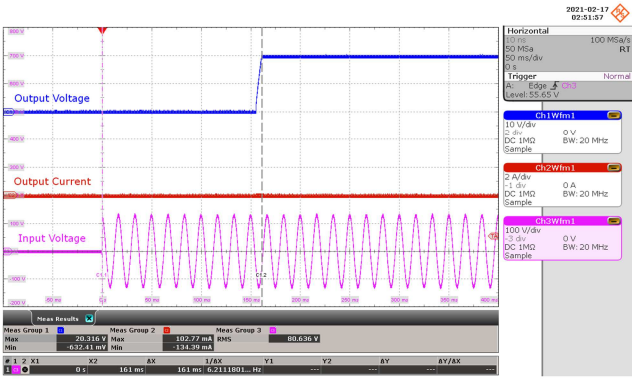

Figure 26 – 90 VAC 60 Hz.
CH1: Output Voltage, 10 V / div., 50 ms / div.
CH2: Output Output Current, 2 A / div., 50 ms / div.
CH3: Input Voltage, 100 V / div., 50 ms / div.
On-Time Delay = 161 ms.

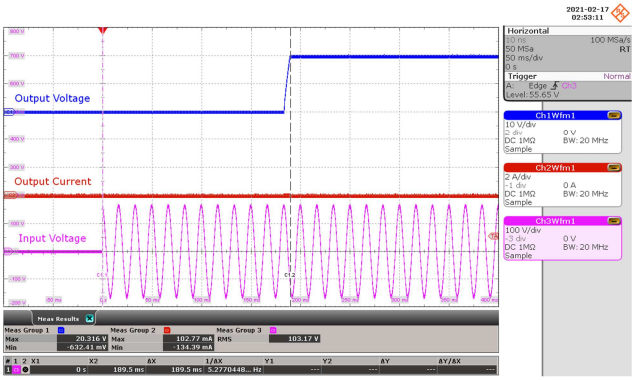

Figure 27 – 115 VAC 60 Hz.
CH1: Output Voltage, 10 V / div., 50 ms / div.
CH2: Output Current, 2 A / div., 50 ms / div.
CH3: Input Voltage, 100 V / div., 50 ms / div.
On-Time Delay = 189.5 ms.

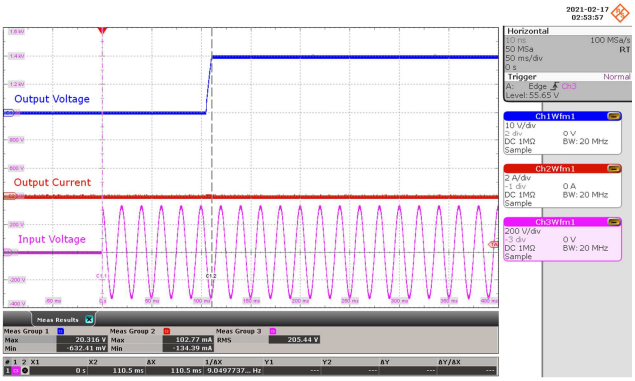

Figure 28 – 230 VAC 60 Hz.
CH1: Output Voltage, 10 V / div., 50 ms / div.
CH2: Output Current, 2 A / div., 50 ms / div.
CH3: Input Voltage, 200 V / div., 50 ms / div.
On-Time Delay = 110.5 ms.

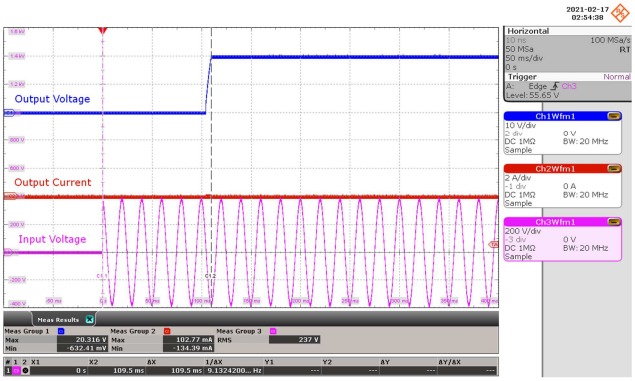

Figure 29 – 265 VAC 60 Hz.
CH1: Output Voltage, 10 V / div., 50 ms / div.
CH2: Output Current, 2 A / div., 50 ms / div.
CH3: Input Voltage, 200 V / div., 50 ms / div.
On-Time Delay = 109.5 ms.

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11.2.2 CR Mode

11.2.2.1 100% Load

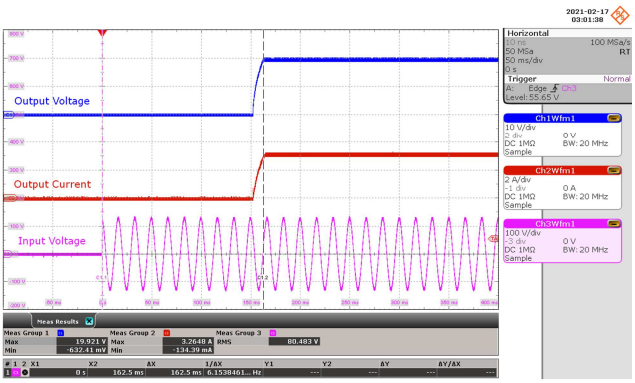

Figure 30 – 90 VAC 60 Hz.
CH1: Output Voltage, 10 V / div., 50 ms / div.
CH2: Output Current, 2 A / div., 50 ms / div.
CH3: Input Voltage, 100 V / div., 50 ms / div.
On-Time Delay = 162.5 ms.

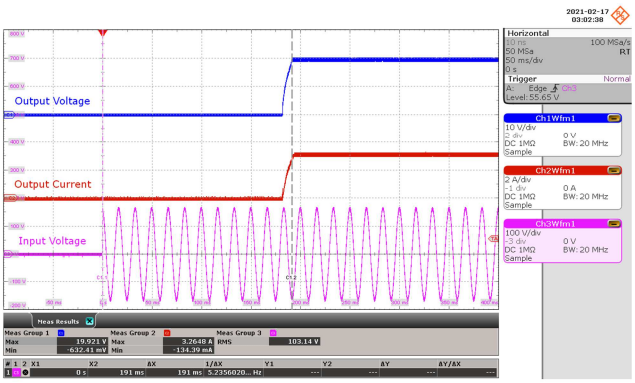

Figure 31 – 115 VAC 60 Hz.
CH1: Output Voltage, 10 V / div., 50 ms / div.
CH2: Output Current, 2 A / div., 50 ms / div.
CH3: Input Voltage, 100 V / div., 50 ms / div.
On-Time Delay = 191 ms.

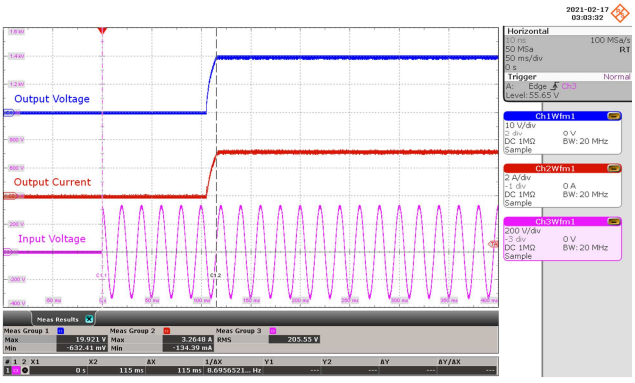

Figure 32 – 230 VAC 60 Hz.
CH1: Output Voltage, 10 V / div., 50 ms / div.
CH2: Output Current, 2 A / div., 50 ms / div.
CH3: Input Voltage, 200 V / div., 50 ms / div.
On-Time Delay = 115 ms.

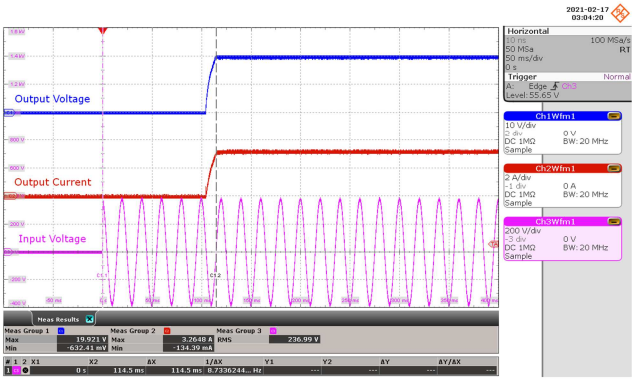

Figure 33 – 265 VAC 60 Hz.
CH1: Output Voltage, 10 V / div., 50 ms / div.
CH2: Output Current, 2 A / div., 50 ms / div.
CH3: Input Voltage, 200 V / div., 50 ms / div.
On-Time Delay = 114.5 ms.

11.1 *MinE-CAP Waveforms*

11.1.1 Normal Operation at 100% Load

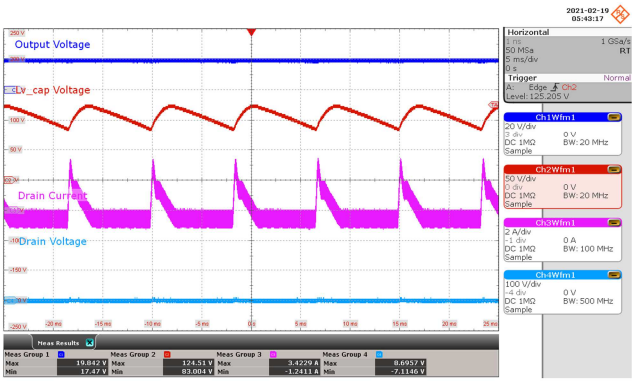

Figure 34 – 90 VAC 60 Hz.
CH1: Output Voltage, 20 V / div., 5 ms / div.
CH2: LV Capacitor Voltage, 50 V / div., 5 ms / div.
CH3: Drain Current, 2 A / div., 5 ms / div.
CH4: Drain Voltage, 100 V / div, 5 ms / div.
V_{LV_CAP} = 124.51 $V_{MAX.}$

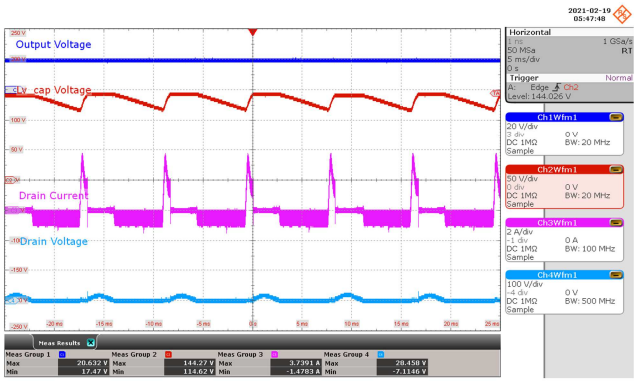

Figure 35 – 115 VAC 60 Hz.
CH1: Output Voltage, 20 V / div., 5 ms / div.
CH2: LV Capacitor Voltage, 50 V / div., 5 ms / div.
CH3: Drain Current, 2 A / div., 5 ms / div.
CH4: Drain Voltage, 100 V / div, 5 ms / div.
V_{LV_CAP} = 144.27 $V_{MAX.}$

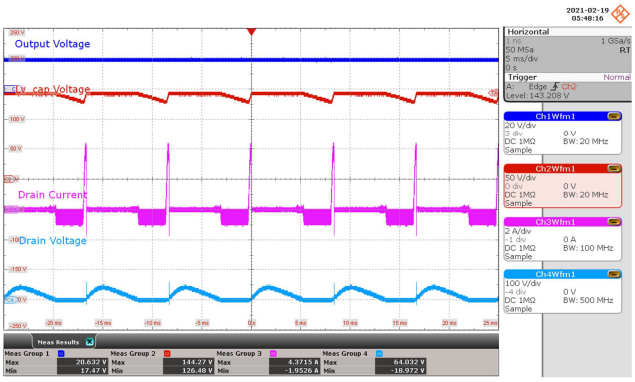

Figure 36 – 132 VAC 60 Hz.
CH1: Output Voltage, 20 V / div., 5 ms / div.
CH2: LV Capacitor Voltage, 50 V / div., 5 ms / div.
CH3: Drain Current, 2 A / div., 5 ms / div.
CH4: Drain Voltage, 100 V / div, 5 ms / div.
V_{LV_CAP} = 144.27 $V_{MAX.}$

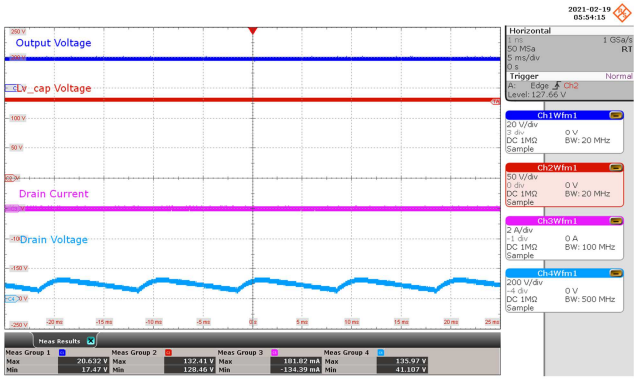

Figure 37 – 180 VAC 60 Hz.
CH1: Output Voltage, 20 V / div., 5 ms / div.
CH2: LV Capacitor Voltage, 50 V / div., 5 ms / div.
CH3: Drain Current, 2 A / div., 5 ms / div.
CH4: Drain Voltage, 200 V / div, 5 ms / div.
V_{LV_CAP} = 132.41 $V_{MAX.}$

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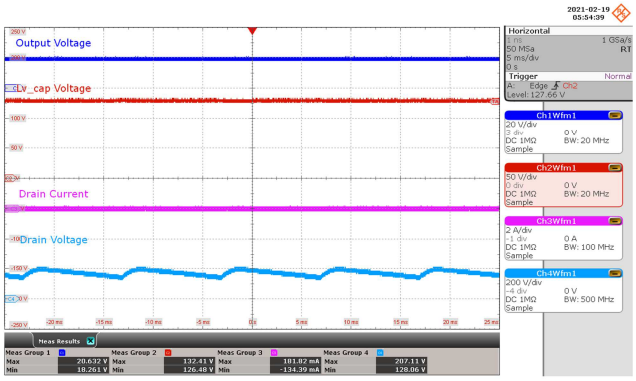

Figure 38 – 230 VAC 60 Hz.
CH1: Output Voltage, 20 V / div., 5 ms / div.
CH2: LV Capacitor Voltage, 50 V / div., 5 ms / div.
CH3: Drain Current, 2 A / div., 5 ms / div.
CH4: Drain Voltage, 200 V / div, 5 ms / div.
V_{LV_CAP} = 132.41 $V_{MAX.}$

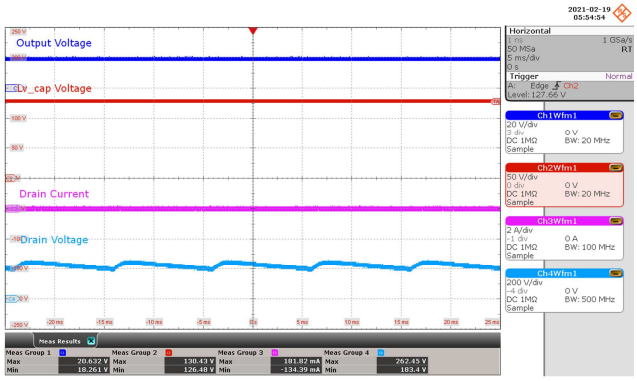

Figure 39 – 265 VAC 60 Hz.
CH1: Output Voltage, 20 V / div., 5 ms / div.
CH2: LV Capacitor Voltage, 50 V / div., 5 ms / div.
CH3: Drain Current, 2 A / div., 5 ms / div.
CH4: Drain Voltage, 200 V / div, 5 ms / div.
V_{LV_CAP} = 130.43 $V_{MAX.}$

11.1.1 Start-up at 100% Load

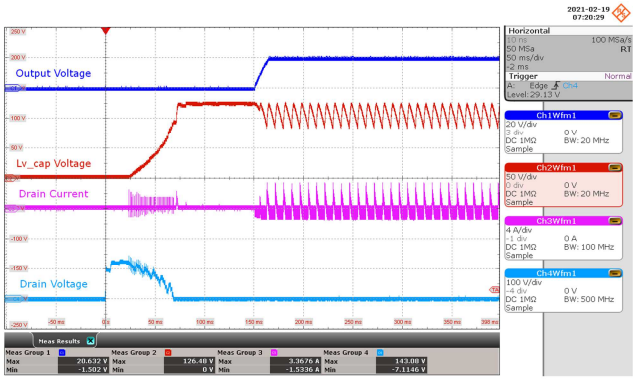

Figure 40 – 90 VAC 60 Hz.
CH1: Output Voltage, 20 V / div., 50 ms / div.
CH2: LV Capacitor Voltage, 50 V / div., 50 ms / div.
CH3: Drain Current, 4 A / div., 50 ms / div.
CH4: Drain Voltage, 100 V / div, 50 ms / div.
V_{LV_CAP} = 126.48 $V_{MAX.}$

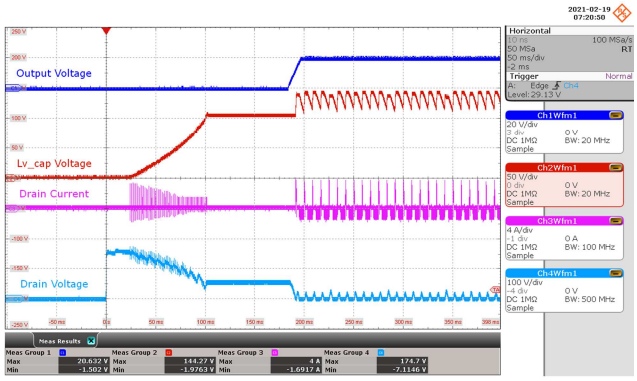

Figure 41 – 115 VAC 60 Hz.
CH1: Output Voltage, 20 V / div., 50 ms / div.
CH2: LV Capacitor Voltage, 50 V / div., 50 ms / div.
CH3: Drain Current, 4 A / div., 50 ms / div.
CH4: Drain Voltage, 100 V / div, 50 ms / div.
V_{LV_CAP} = 144.27 $V_{MAX.}$

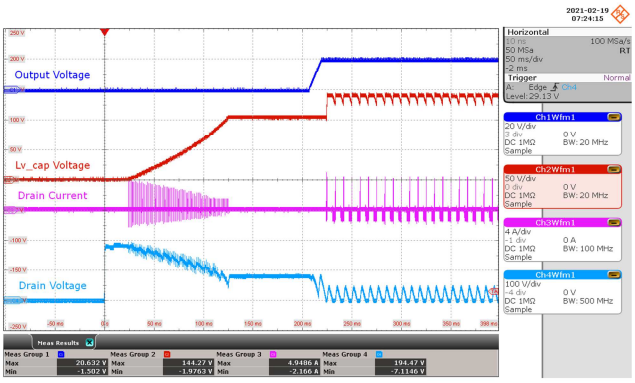

Figure 42 – 132 VAC 60 Hz.
CH1: Output Voltage, 20 V / div., 50 ms / div.
CH2: LV Capacitor Voltage, 50 V / div., 50 ms / div.
CH3: Drain Current, 4 A / div., 50 ms / div.
CH4: Drain Voltage, 100 V / div, 50 ms / div.
V_{LV_CAP} = 144.27 $V_{MAX.}$

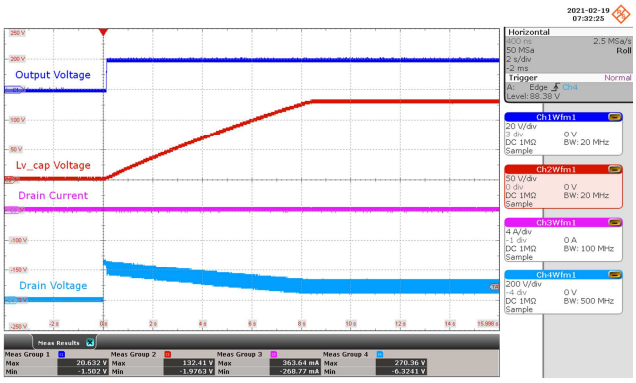

Figure 43 – 180 VAC 60 Hz.
CH1: Output Voltage, 20 V / div., 2 s / div.
CH2: LV Capacitor Voltage, 50 V / div., 2 s / div.
CH3: Drain Current, 4 A / div., 2 s / div.
CH4: Drain Voltage, 200 V / div, 2 s / div.
V_{LV_CAP} = 132.41 V_{MAX}

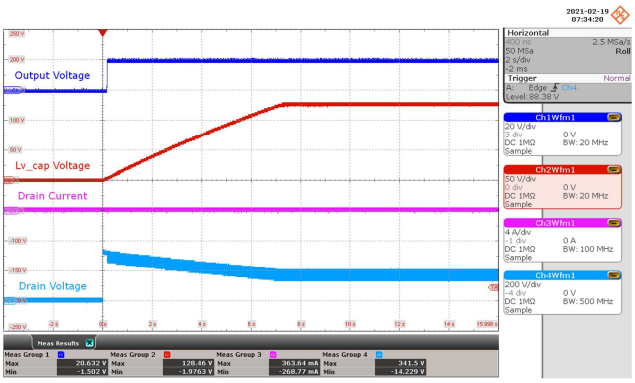

Figure 44 – 230 VAC 60 Hz.
CH1: Output Voltage, 20 V / div., 2 s / div.
CH2: LV Capacitor Voltage, 50 V / div., 2 s / div.
CH3: Drain Current, 4 A / div., 2 s / div.
CH4: Drain Voltage, 200 V / div, 2 s / div.
V_{LV_CAP} = 128.46 $V_{MAX.}$

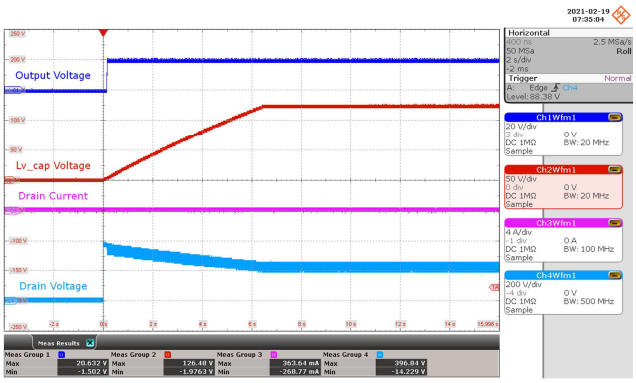

Figure 45 – 265 VAC 60 Hz.
CH1: Output Voltage, 20 V / div., 2 s / div.
CH2: LV Capacitor Voltage, 50 V / div., 2 s / div.
CH3: Drain Current, 4 A / div., 2 s / div.
CH4: Drain Voltage, 200 V / div, 2 s / div.
V_{LV_CAP} = 126.48 $V_{MAX.}$

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11.2 *Switching Waveforms*

11.2.1 Primary MOSFET Drain-Source Voltage and Current at Normal Operation

11.2.1.1 100% Load

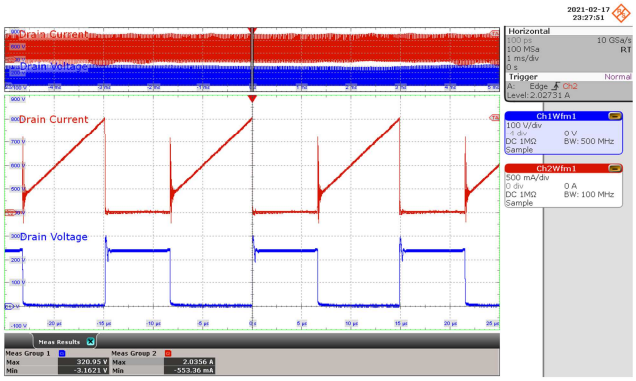

Figure 46 – 90 VAC 60 Hz.
CH1: Drain Voltage, 100 V / div., 1 ms / div.
CH2: Drain Current, 500 mA / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 320.95 V, $I_{DS(MAX)}$ = 2.0356 A.

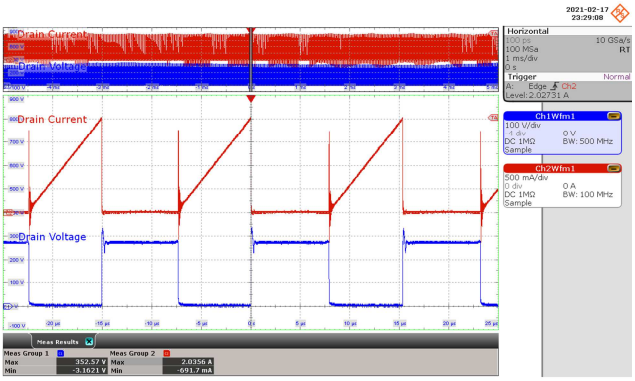

Figure 47 – 115 VAC 60 Hz.
CH1: Drain Voltage, 100 V / div., 1 ms / div.
CH2: Drain Current, 500 mA / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 352.57 V, $I_{DS(MAX)}$ = 2.0356 A.

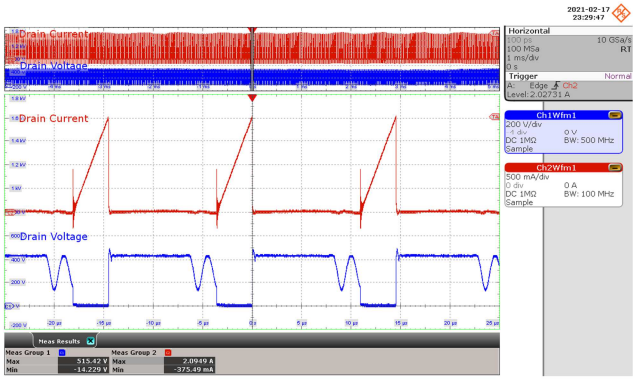

Figure 48 – 230 VAC 60 Hz.
CH1: Drain Voltage, 200 V / div., 1 ms / div.
CH2: Drain Current, 500 mA / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 515.42 V, $I_{DS(MAX)}$ = 2.0949 A.

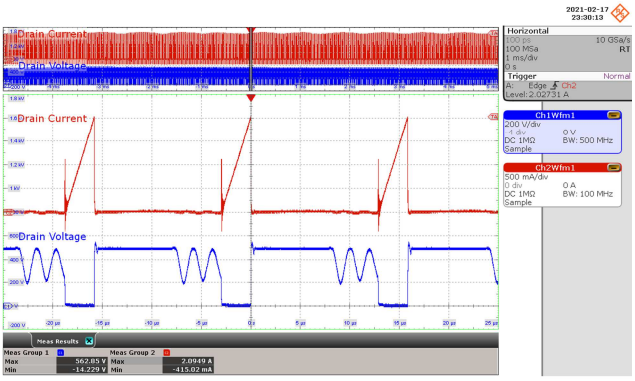

Figure 49 – 265 VAC 60 Hz.
CH1: Drain Voltage, 200 V / div., 1 ms / div.
CH2: Drain Current, 500 mA / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 562.85 V, $I_{DS(MAX)}$ = 2.0949 A.

11.2.1.2 0% Load

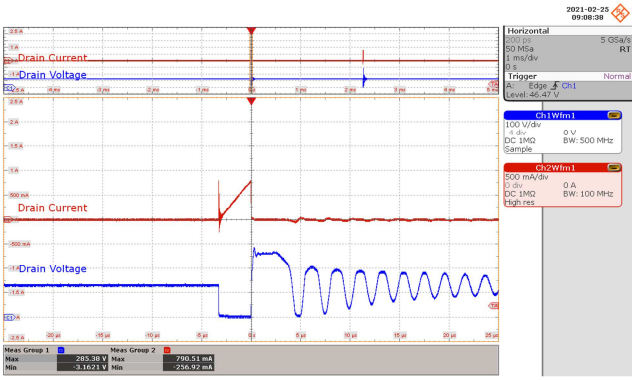

Figure 50 – 90 VAC 60 Hz.
CH1: V_{DS}, 100 V / div., 1 ms / div.
CH2: I_{DS}, 500 mA / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 285.38 V, $I_{DS(MAX)}$ = 790.51 mA.

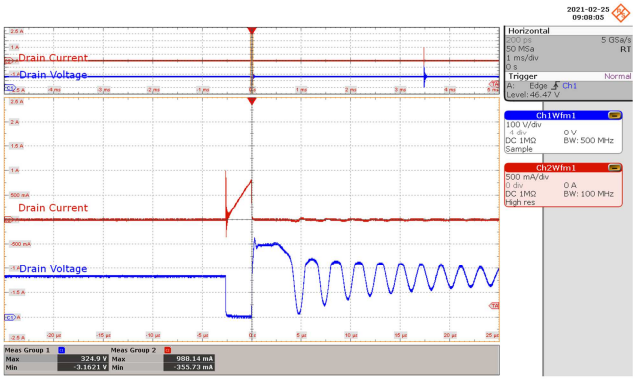

Figure 51 – 115 VAC 60 Hz.
CH1: V_{DS}, 100 V / div., 1 ms / div.
CH2: I_{DS}, 500 mA / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 324.9 V, $I_{DS(MAX)}$ = 988.14 mA.

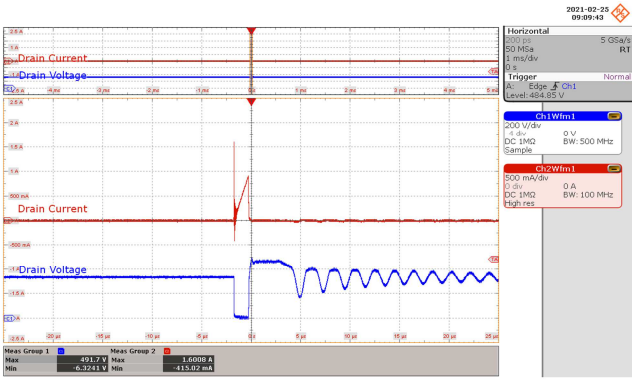

Figure 52 – 230 VAC 60 Hz.
CH1: V_{DS}, 200 V / div., 1 ms / div.
CH2: I_{DS}, 500 mA / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 491.7 V, $I_{DS(MAX)}$ = 1.6008 A.

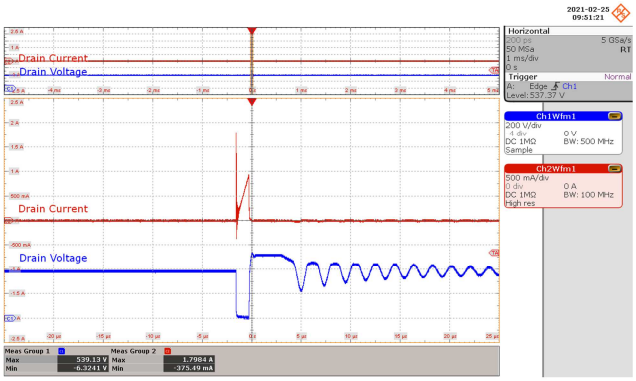

Figure 53 – 265 VAC 60 Hz.
CH1: V_{DS}, 200 V / div., 1 ms / div.
CH2: I_{DS}, 500 mA / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 539.13 V, $I_{DS(MAX)}$ = 1.7984 A.

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11.2.2 Primary MOSFET Drain-Source Voltage and Current at Start-up Operation

11.2.2.1 100% Load

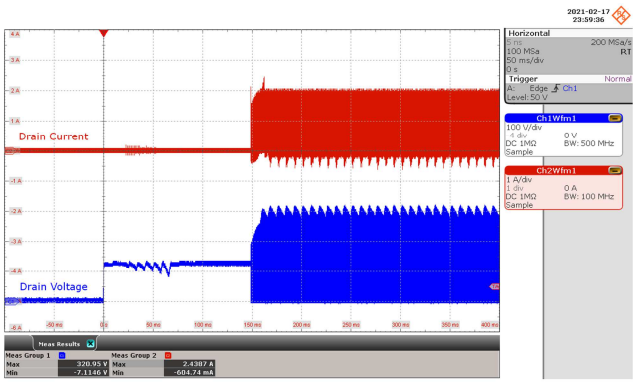

Figure 54 – 90 VAC 60 Hz.
CH1: Drain Voltage, 100 V / div., 50 ms / div.
CH2: Drain Current, 1 A / div., 50 ms / div.
$V_{DS(MAX)}$ = 320.95 V, $I_{DS(MAX)}$ = 2.4387 A.

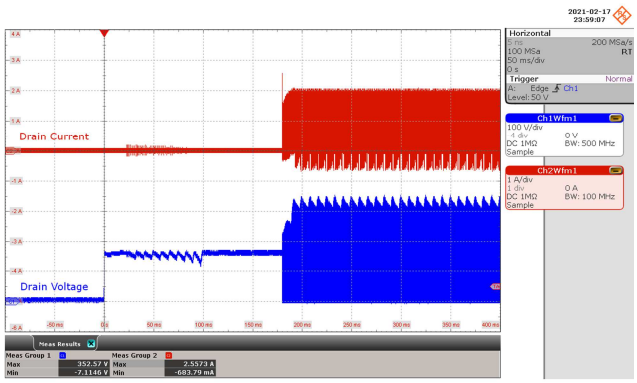

Figure 55 – 115 VAC 60 Hz.
CH1: Drain Voltage, 100 V / div., 50 ms / div.
CH2: Drain Current, 1 A / div., 50 ms / div.
$V_{DS(MAX)}$ = 352.57 V, $I_{DS(MAX)}$ = 2.5573 A.

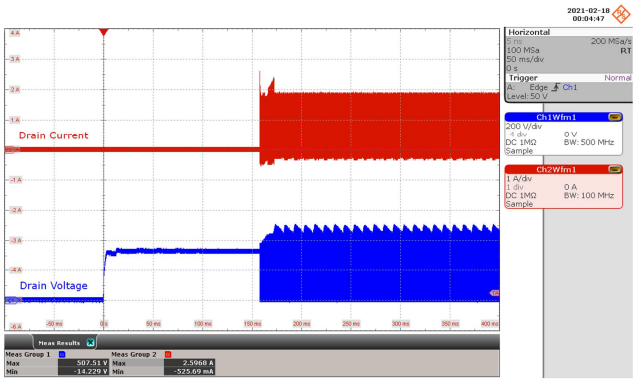

Figure 56 – 230 VAC 60 Hz.
CH1: Drain Voltage, 200 V / div., 50 ms / div.
CH2: Drain Current, 1 A / div., 50 ms / div.
$V_{DS(MAX)}$ = 507.51 V, $I_{DS(MAX)}$ = 2.5968 A.

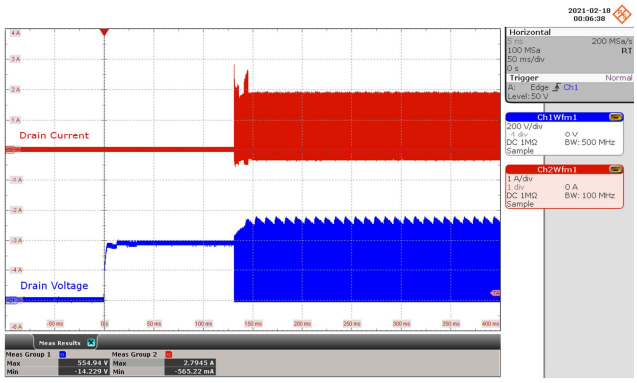

Figure 57 – 265 VAC 60 Hz.
CH1: Drain Voltage, 200 V / div., 50 ms / div.
CH2: Drain Current, 1 A / div., 50 ms / div.
$V_{DS(MAX)}$ = 554.94 V, $I_{DS(MAX)}$ = 2.7945 A.

11.2.2.2 0% Load

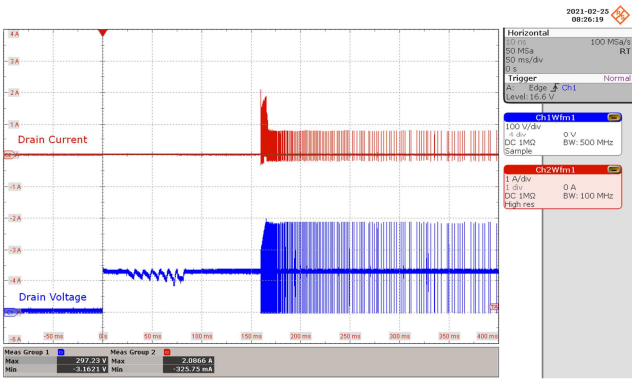

Figure 58 – 90 VAC 60 Hz.
CH1: V_{DS}, 100 V / div., 50 ms / div.
CH2: I_{DS}, 1 A / div., 50 ms / div.
$V_{DS(MAX)}$ = 297.23 V, $I_{DS(MAX)}$ = 2.0866 A.

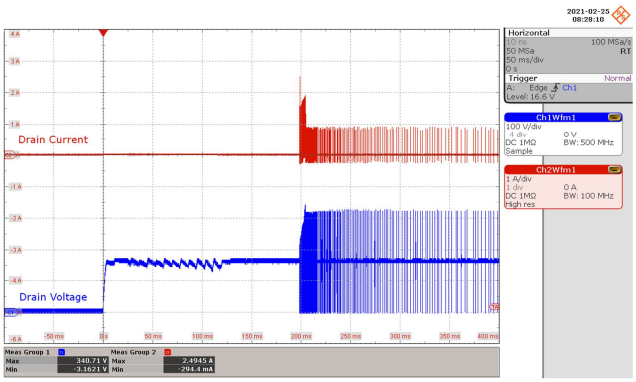

Figure 59 – 115 VAC 60 Hz.
CH1: V_{DS}, 100 V / div., 50 ms / div.
CH2: I_{DS}, 1 A / div., 50 ms / div.
$V_{DS(MAX)}$ = 340.71 V, $I_{DS(MAX)}$ = 2.4945 A.

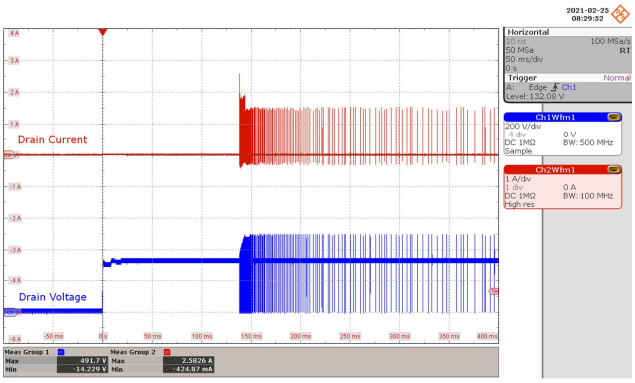

Figure 60 – 230 VAC 60 Hz.
CH1: V_{DS}, 200 V / div., 50 ms / div.
CH2: I_{DS}, 1 A / div., 50 ms / div.
$V_{DS(MAX)}$ = 491.7 V, $I_{DS(MAX)}$ = 2.5826 A

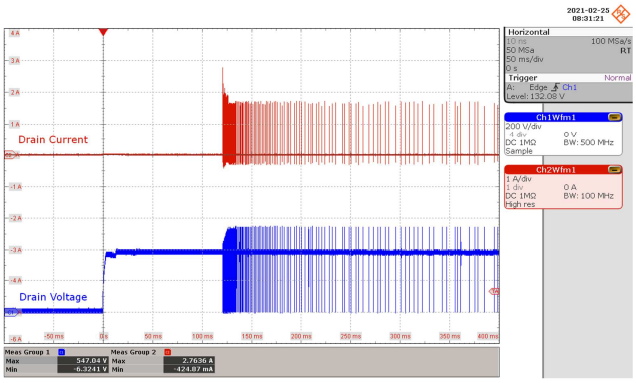

Figure 61 – 265 VAC 60 Hz.
CH1: V_{DS}, 200 V / div., 50 ms / div.
CH2: I_{DS}, 1 A / div., 50 ms / div.
$V_{DS(MAX)}$ = 547.04 V, $I_{DS(MAX)}$ = 2.7636 A.

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11.2.3 SR FET Voltage and Current at Normal Operation

11.2.3.1 100% Load

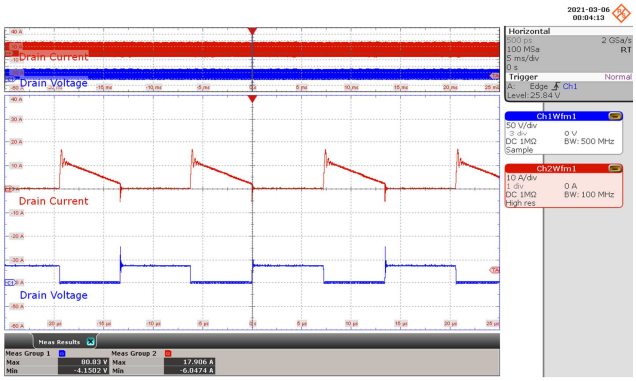

Figure 62 – 90 VAC 60 Hz.
CH1: SR FET Drain Voltage, 50 V / div., 5 ms / div.
CH2: SR FET Drain Current, 10 A / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 80.83 V, $I_{DS(MAX)}$ = 17.906 A.

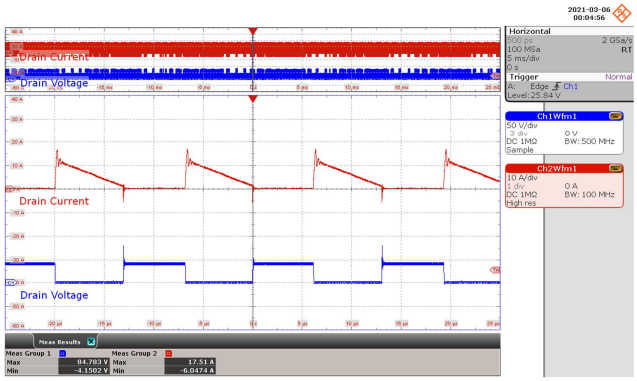

Figure 63 – 115 VAC 60 Hz.
CH1: SR FET Drain Voltage, 50 V / div., 5 ms / div.
CH2: SR FET Drain Current, 10 A / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 84.783 V, $I_{DS(MAX)}$ = 17.51 A.

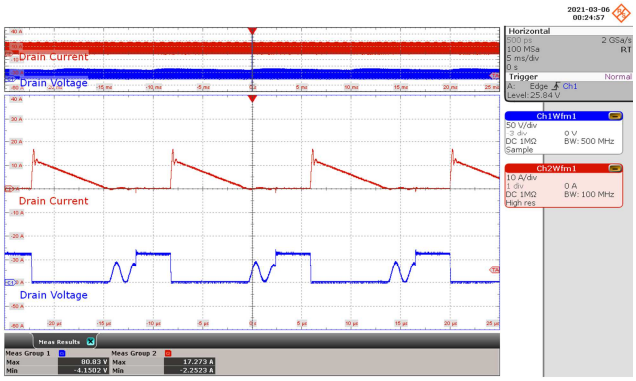

Figure 64 – 230 VAC 60 Hz.
CH1: SR FET Drain Voltage, 50 V / div., 5 ms / div.
CH2: SR FET Drain Current, 10 A / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 80.83 V, $I_{DS(MAX)}$ = 17.273 A.

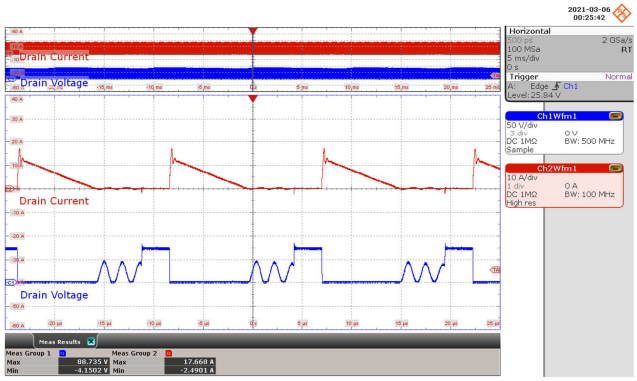

Figure 65 – 265 VAC 60 Hz.
CH1: SR FET Drain Voltage, 50 V / div., 5 ms / div.
CH2: SR FET Drain Current, 10 A / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 88.735 V, $I_{DS(MAX)}$ = 17.668 A.

11.2.3.2 0% Load

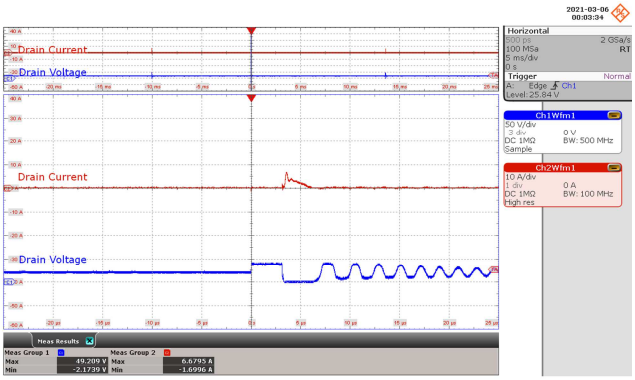

Figure 66 – 90 VAC 60 Hz.
CH1: V_{DS}, 50 V / div., 5 ms / div.
CH2: I_{DS}, 10 A / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 49.209 V, $I_{DS(MAX)}$ = 6.6795 A.

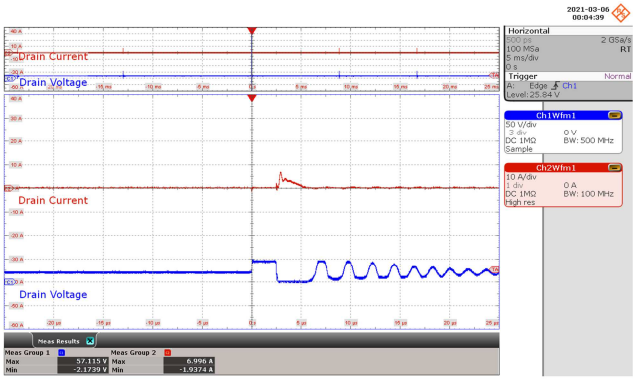

Figure 67 – 115 VAC 60 Hz.
CH1: V_{DS}, 50 V / div., 5 ms / div.
CH2: I_{DS}, 10 A / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 57.115 V, $I_{DS(MAX)}$ = 6.996 A.

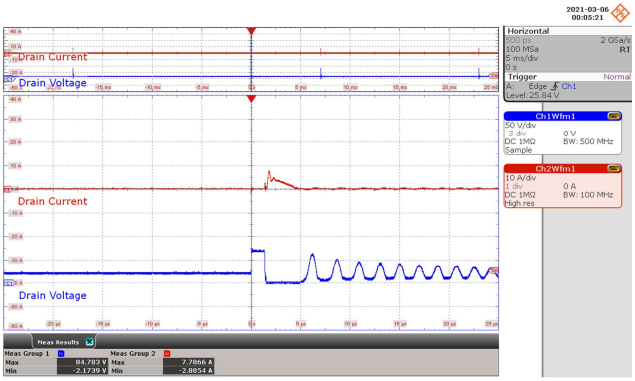

Figure 68 – 230 VAC 60 Hz.
CH1: V_{DS}, 50 V / div., 5 ms / div.
CH2: I_{DS}, 10 A / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 84.783 V, $I_{DS(MAX)}$ = 7.7866 A

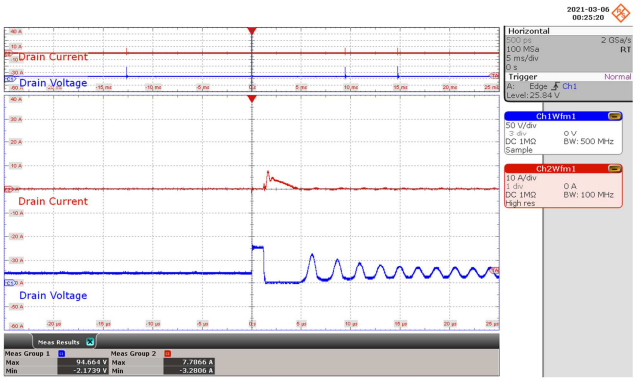

Figure 69 – 265 VAC 60 Hz.
CH1: V_{DS}, 50 V / div., 5 ms / div.
CH2: I_{DS}, 10 A / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 94.664 V, $I_{DS(MAX)}$ = 7.7866 A.

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11.2.4 SR FET Voltage and Current at Start-up Operation

11.2.4.1 100% Load

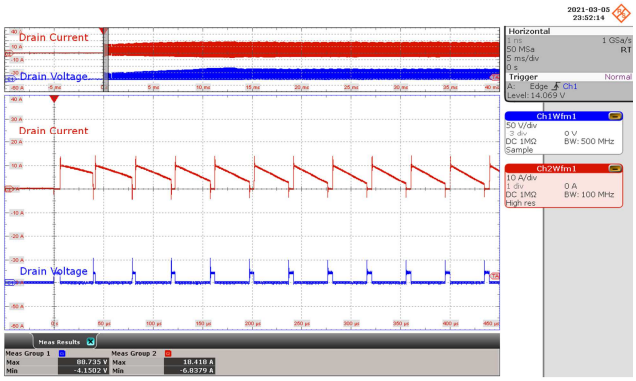

Figure 70 – 90 VAC 60 Hz.
CH1: SR FET Drain Voltage, 50 V / div., 5 ms / div.
CH2: SR FET Drain Current, 10 A / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 88.735 V, $I_{DS(MAX)}$ = 18.418 A.

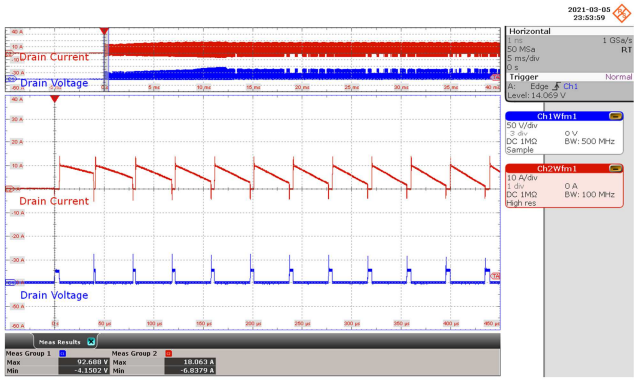

Figure 71 – 115 VAC 60 Hz.
CH1: SR FET Drain Voltage, 50 V / div., 5 ms / div.
CH2: SR FET Drain Current, 10 A / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 92.688 V, $I_{DS(MAX)}$ = 18.063 A.

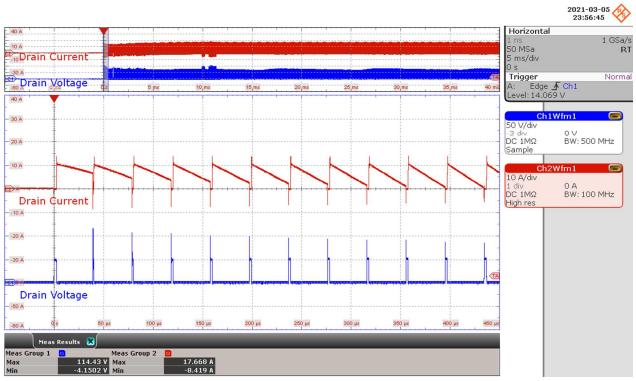

Figure 72 – 230 VAC 60 Hz.
CH1: SR FET Drain Voltage, 50 V / div., 5 ms / div.
CH2: SR FET Drain Current, 10 A / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 114.43 V, $I_{DS(MAX)}$ = 17.668 A.

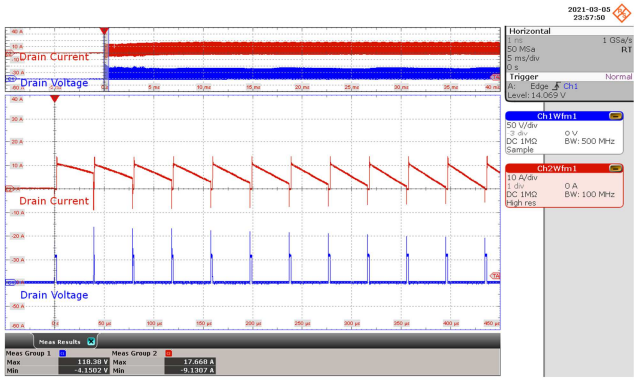

Figure 73 – 265 VAC 60 Hz.
CH1: SR FET Drain Voltage, 50 V / div., 5 ms / div.
CH2: SR FET Drain Current, 10 A / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 118.38 V, $I_{DS(MAX)}$ = 17.668 A.

11.2.4.2 0% Load

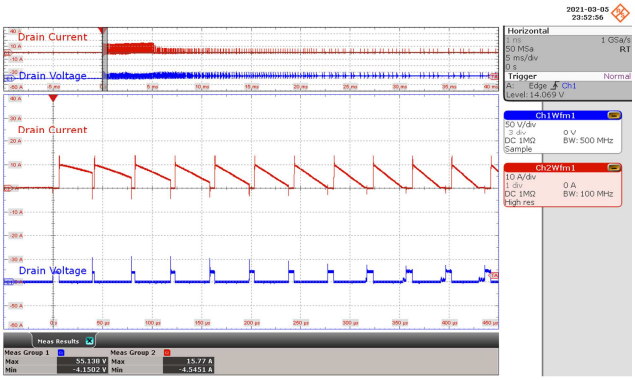

Figure 74 – 90 VAC 60 Hz.
CH1: V_{DS}, 50 V / div., 5 ms / div.
CH2: I_{DS}, 10 A / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 55.138 V, $I_{DS(MAX)}$ = 15.77 A.

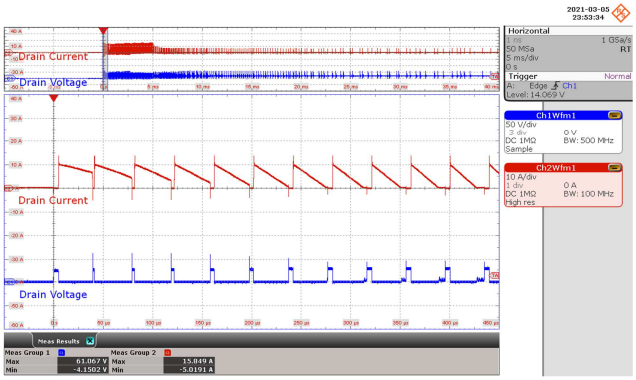

Figure 75 – 115 VAC 60 Hz.
CH1: V_{DS}, 50 V / div., 5 ms / div.
CH2: I_{DS}, 10 A / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 61.067 V, $I_{DS(MAX)}$ = 15.849 A.

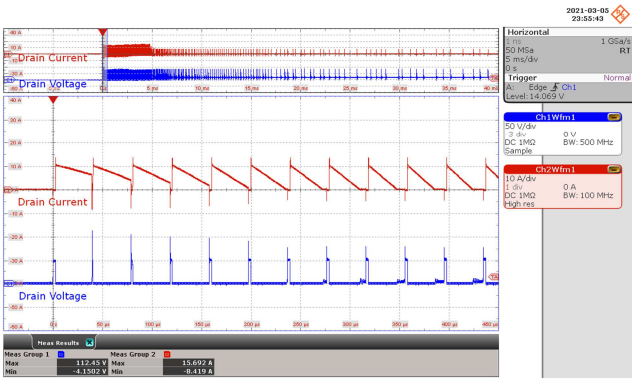

Figure 76 – 230 VAC 60 Hz.
CH1: V_{DS}, 50 V / div., 5 ms / div.
CH2: I_{DS}, 10 A / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 112.45 V, $I_{DS(MAX)}$ = 15.692 A.

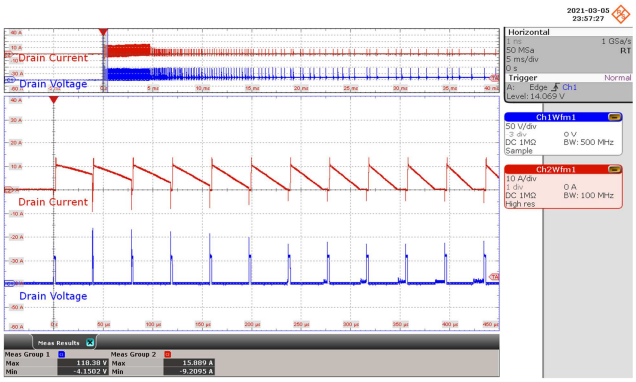

Figure 77 – 265 VAC 60 Hz.
CH1: V_{DS}, 50 V / div., 5 ms / div.
CH2: I_{DS}, 10 A / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 118.38 V, $I_{DS(MAX)}$ = 15.889 A.

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11.3 ***Fault Condition***

11.3.1 Output Short-Circuit

Test Condition: Short circuit applied at the end of PCB during start-up

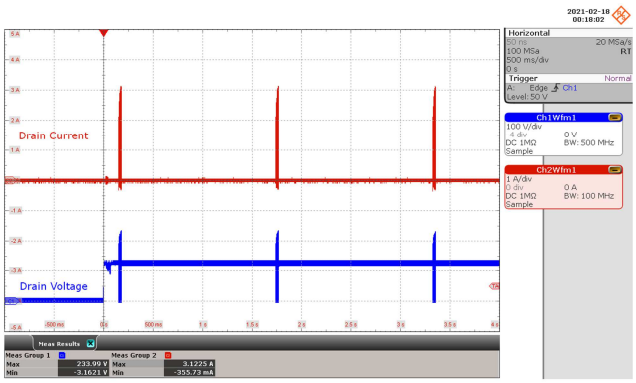

Figure 78 – 90 VAC 60 Hz.
CH1: Drain Voltage, 100 V / div., 500 ms / div.
CH2: Drain Current, 1 A / div., 500 ms / div.
$V_{DS(MAX)}$ = 233.99 V, $I_{DS(MAX)}$ = 3.1225 A.

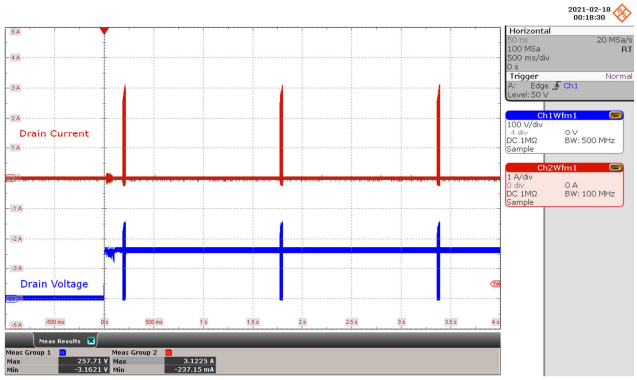

Figure 79 – 115 VAC 60 Hz.
CH1: Drain Voltage, 100 V / div., 500 ms / div.
CH2: Drain Current, 1 A / div., 500 ms / div.
$V_{DS(MAX)}$ = 257.71 V, $I_{DS(MAX)}$ = 3.1225 A.

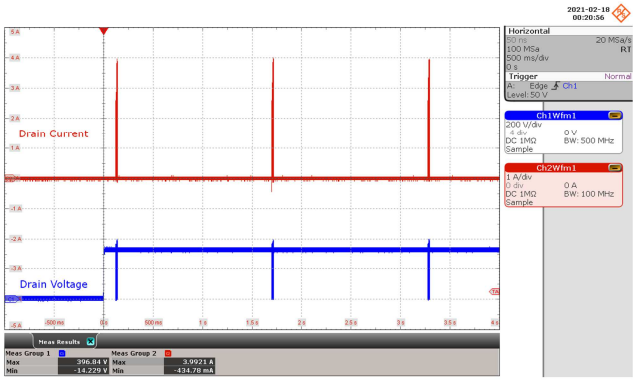

Figure 80 – 230 VAC 60 Hz.
CH1: Drain Voltage, 200 V / div., 500 ms / div.
CH2: Drain Current, 1 A / div., 500 ms / div.
$V_{DS(MAX)}$ = 396.84 V, $I_{DS(MAX)}$ = 3.9921 A.

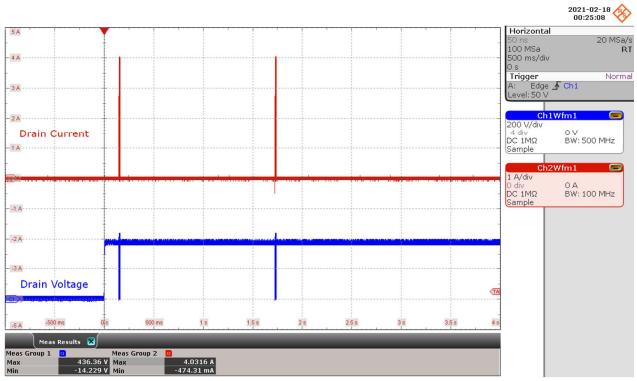

Figure 81 – 265 VAC 60 Hz.
CH1: Drain Voltage, 200 V / div., 500 ms / div.
CH2: Drain Current, 1 A / div., 500 ms / div.
$V_{DS(MAX)}$ = 436.36 V, $I_{DS(MAX)}$ = 4.0316 A.

11.4 ***Output Voltage Ripple***

11.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V X7R ceramic type and one (1) 47 μF / 25 V aluminum electrolytic KZE series from Nippon Chemi-Con. It is recommended to make the capacitor leads as short as possible so as to further reduce the magnitude of spurious signals. The aluminum electrolytic type capacitor is also polarized, so proper polarity across DC outputs must be maintained (see below).

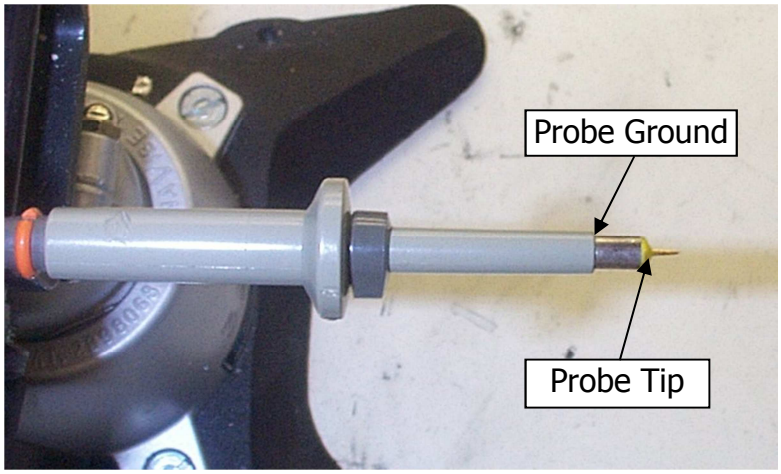

Figure 82 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

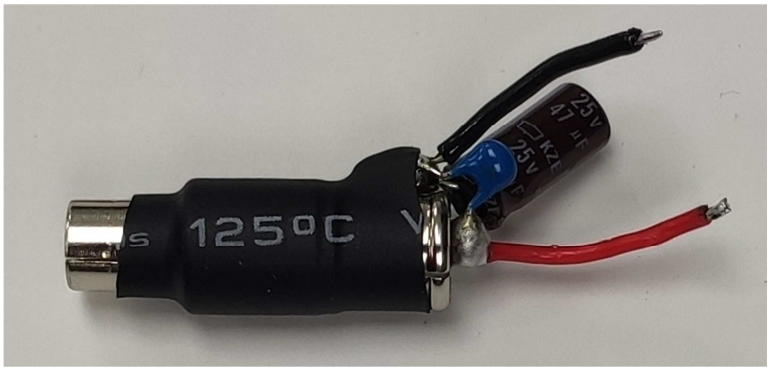

Figure 83 –Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

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11.4.2 Measurement Results

Note: All ripple measurements were taken at the end of PCB.

11.4.2.1 100% Load Condition

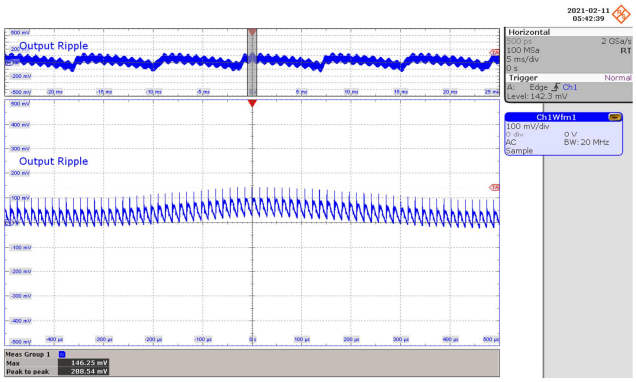

Figure 84 – 90 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 288.54 mV.

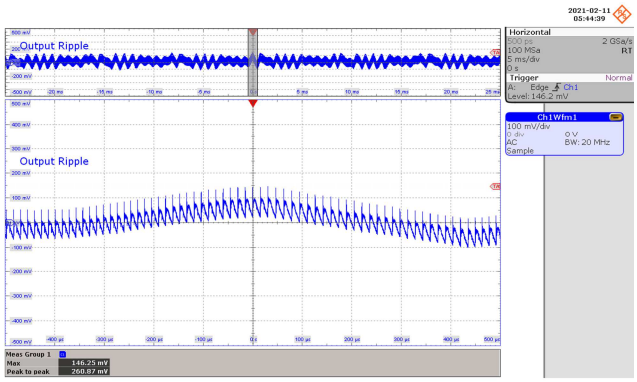

Figure 85 – 115 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 260.87 mV.

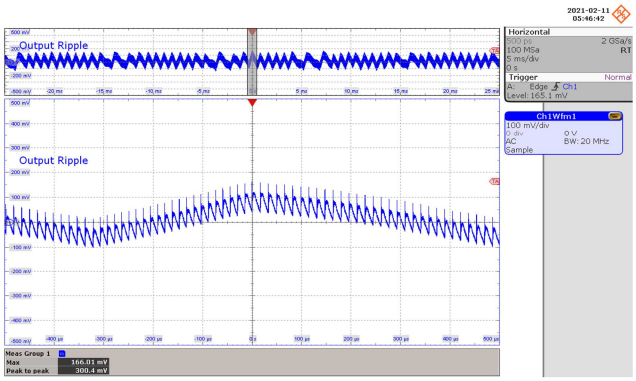

Figure 86 – 230 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 300.4 mV.

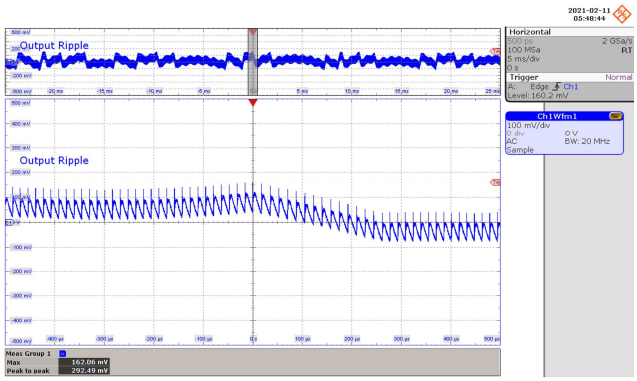

Figure 87 – 265 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 292.49 mV.

11.4.2.2 75% Load Condition

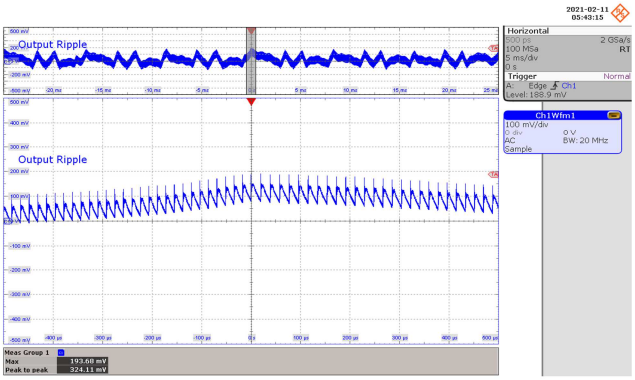

Figure 88 – 90 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 324.11 mV.

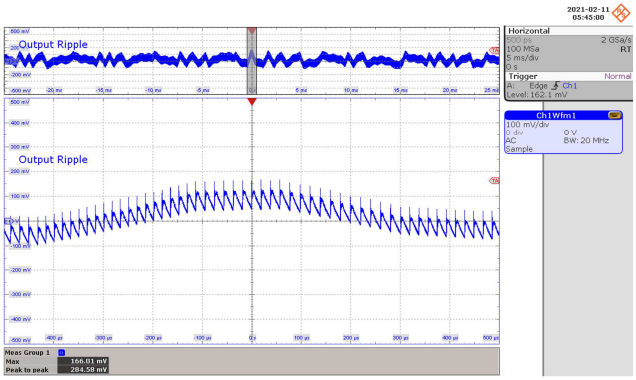

Figure 89 – 115 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 284.58 mV.

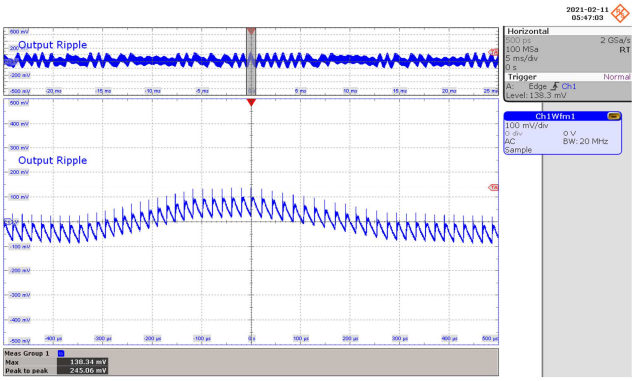

Figure 90 – 230 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 245.06 mV.

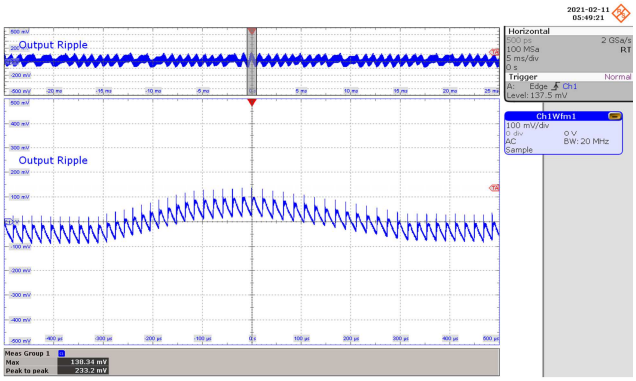

Figure 91 – 265 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 233.2 mV.

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11.4.2.3 50% Load Condition

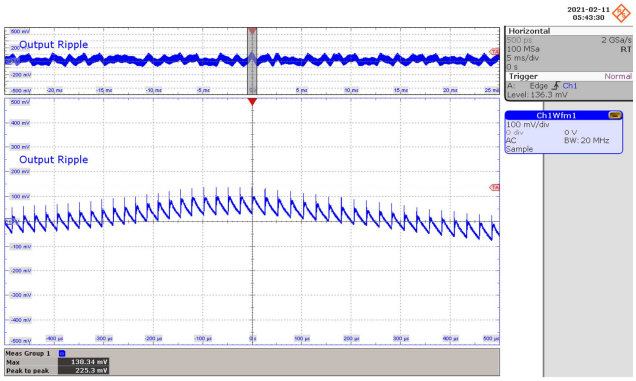

Figure 92 – 90 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 225.3 mV.

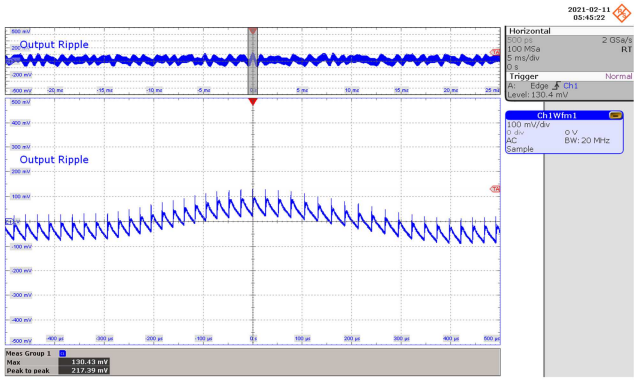

Figure 93 – 115 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 217.39 mV.

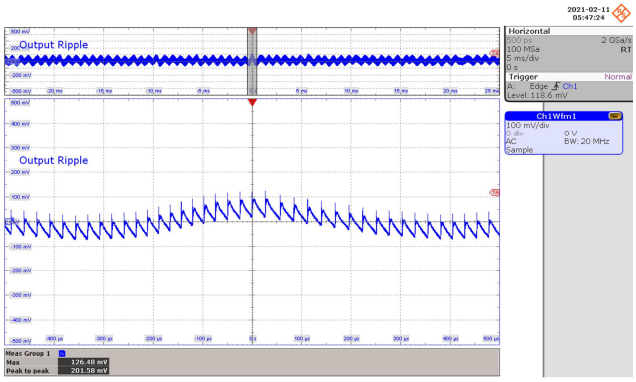

Figure 94 – 230 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 201.58 mV.

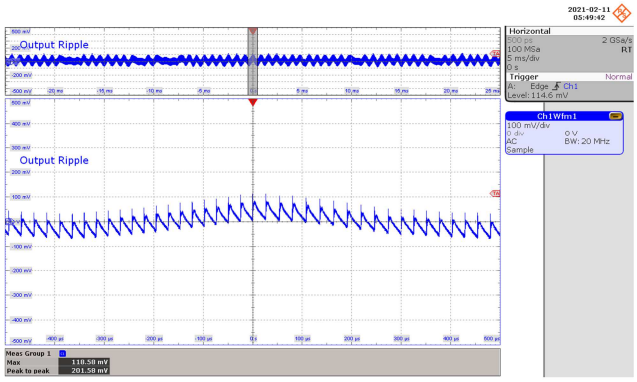

Figure 95 – 265 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 201.58 mV.

11.4.2.4 25% Load Condition

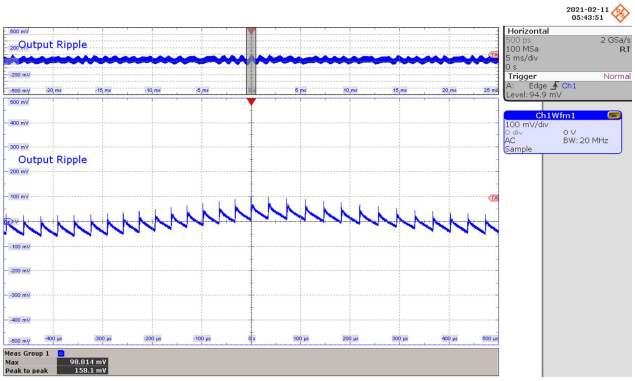

Figure 96 – 90 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 158.1 mV.

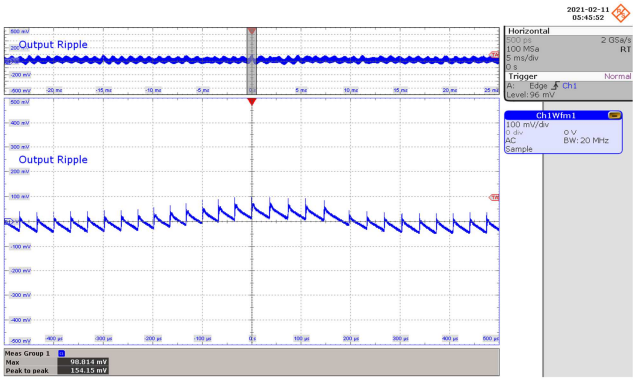

Figure 97 – 115 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 154.15 mV.

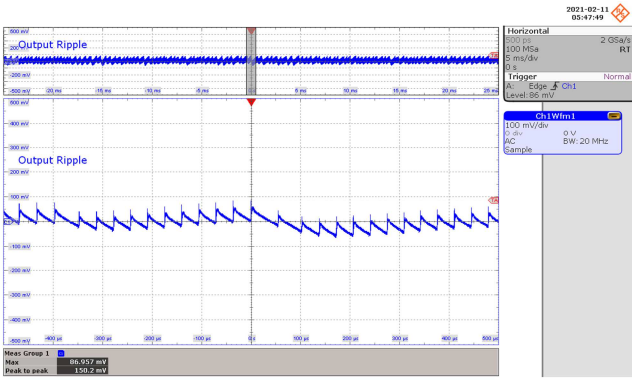

Figure 98 – 230 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 150.2 mV.

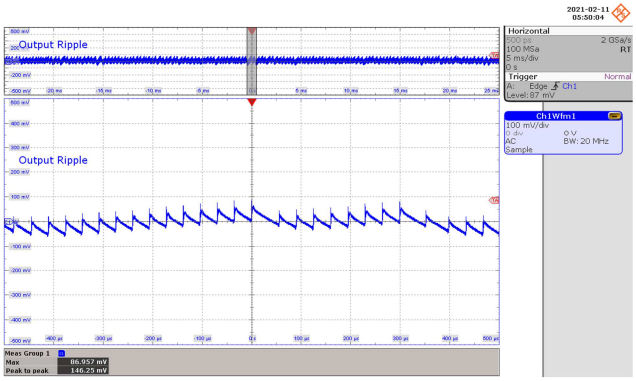

Figure 99 – 265 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 146.25 mV.

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11.4.2.5 0% Load Condition

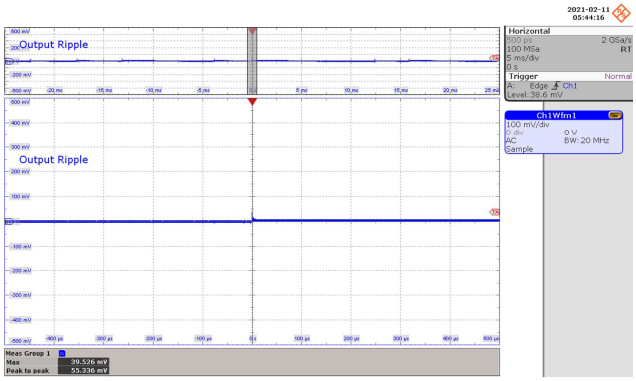

Figure 100 – 90 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 55.336 mV.

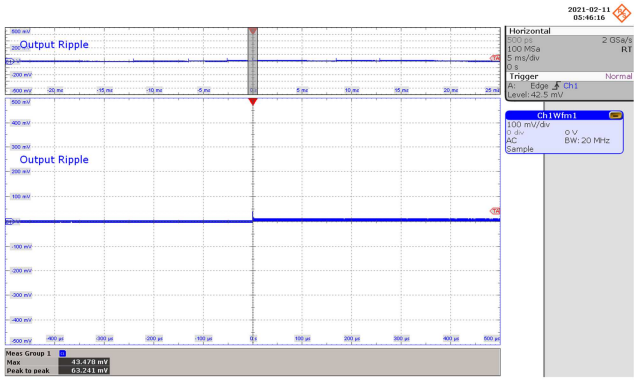

Figure 101 – 115 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 63.241 mV.

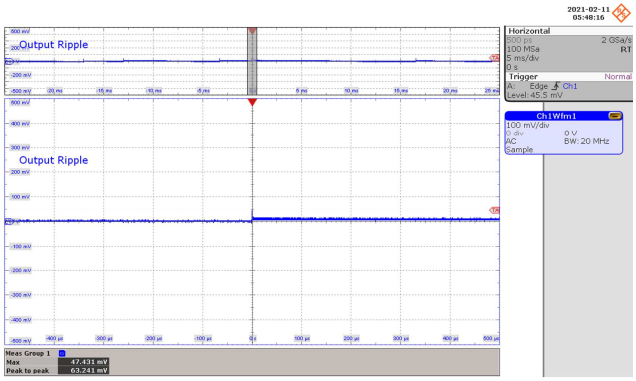

Figure 102 – 230 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 63.241 mV.

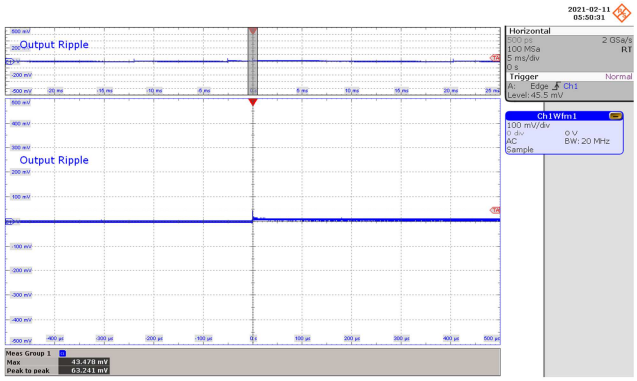

Figure 103 – 265 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 63.241 mV.

11.4.3 Output Ripple Voltage Graph from 0% - 100%

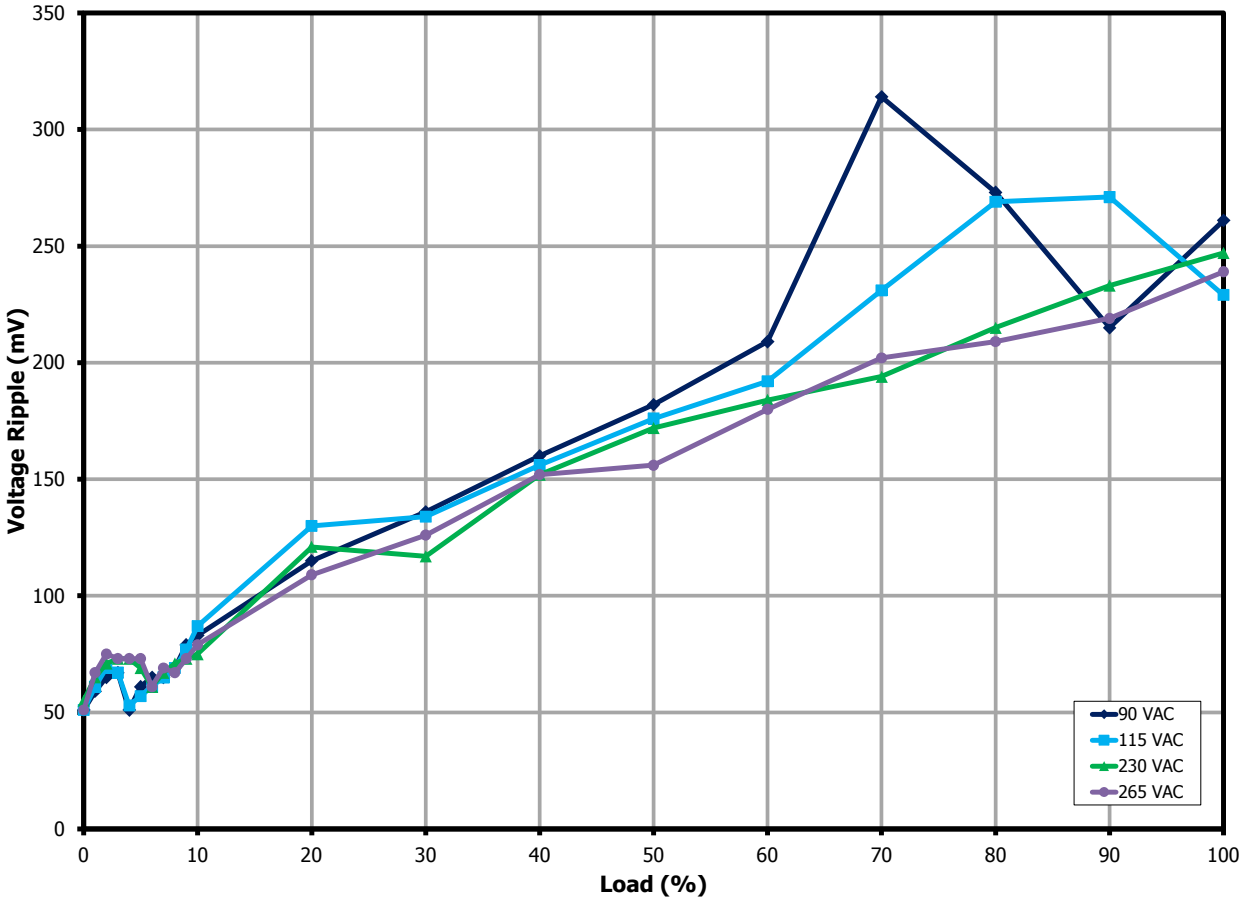

Figure 104 – Output Ripple Voltage Measured at End of PCB (Room Temperature).

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12 Thermal Performance

12.1 *Test Set-Up*

Thermal evaluation was performed under two conditions: (1) room temperature and (2), 40 ºC ambient inside a thermal chamber. In both conditions, the circuit is soaked for at least an hour under full load conditions.

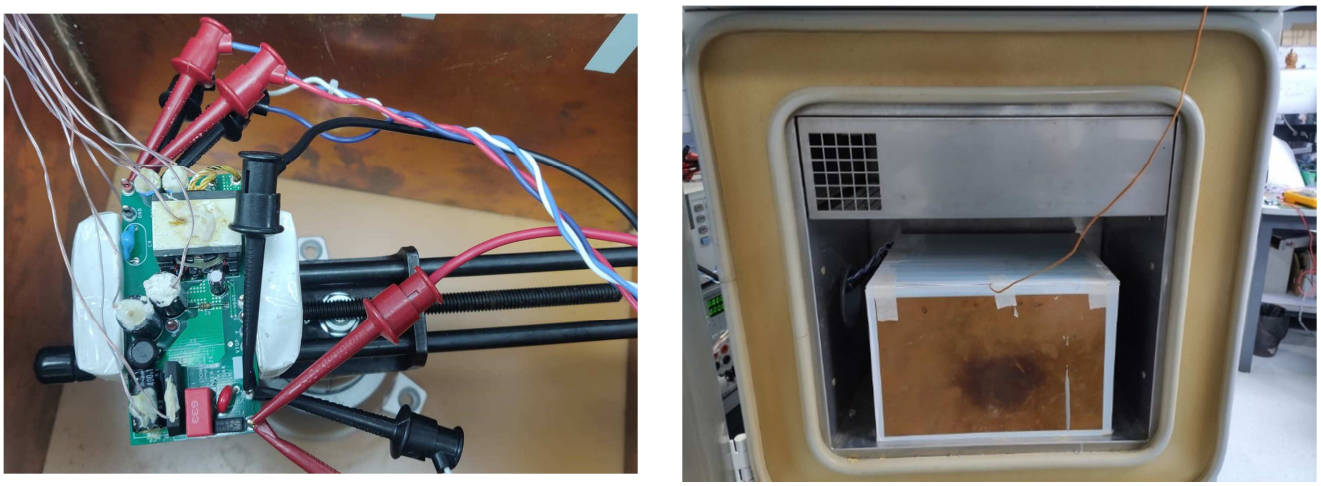

Figure 105 – Thermal Performance Set-up Using Thermal Chamber.

12.2 *Thermal Performance at Room Temperature*

12.2.1 90 VAC at Room Temperature and Full Load

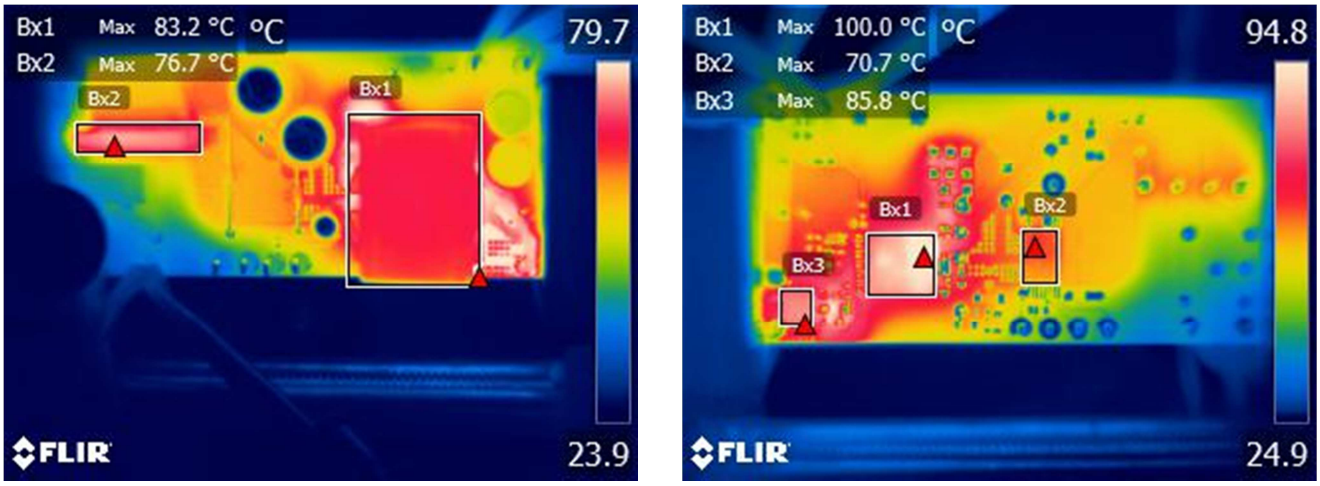

Figure 106 – Thermal Performance at 90 VAC.

Component	Temperature (°C)
Ambient	24.9
SR FET (Q1)	85.8
INN3679C (U2)	100.0
MinE-CAP (U1)	70.7
Transformer (T1)	83.2
Bridge (BR1)	76.7

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12.2.2 265 VAC at Room Temperature and Full Load

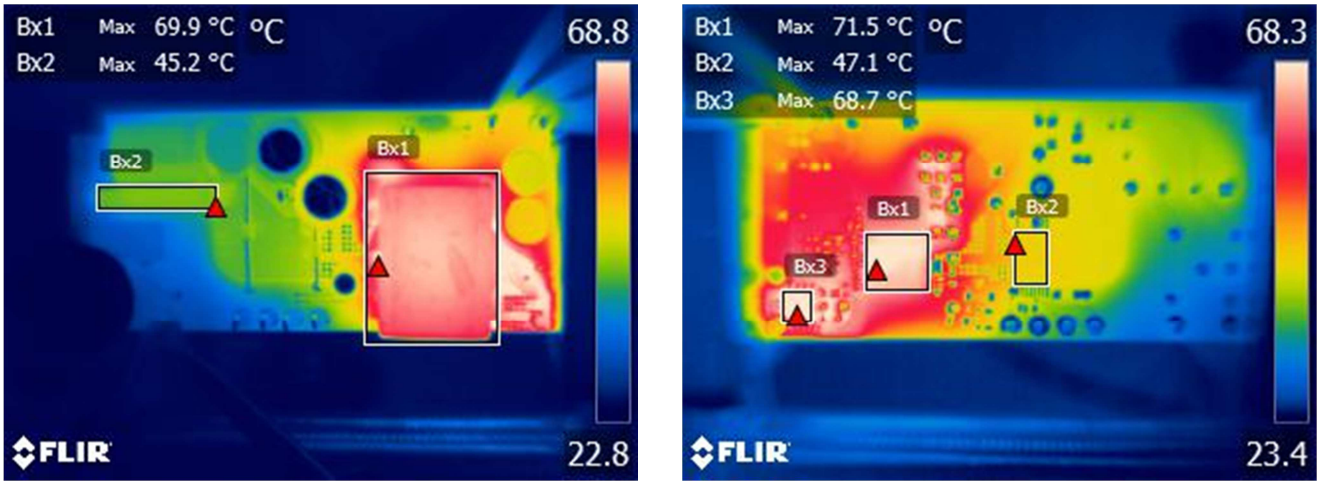

Figure 107 – Thermal Performance at 265 VAC.

Component	Temperature (°C)
Ambient	23.4
SR FET (Q1)	68.7
INN3679C (U2)	71.5
MinE-CAP (U1)	47.1
Transformer (T1)	69.9
Bridge (BR1)	45.2

12.3 *Thermal Performance at 40 °C*

12.3.1 90 VAC Full Load at 40 °C

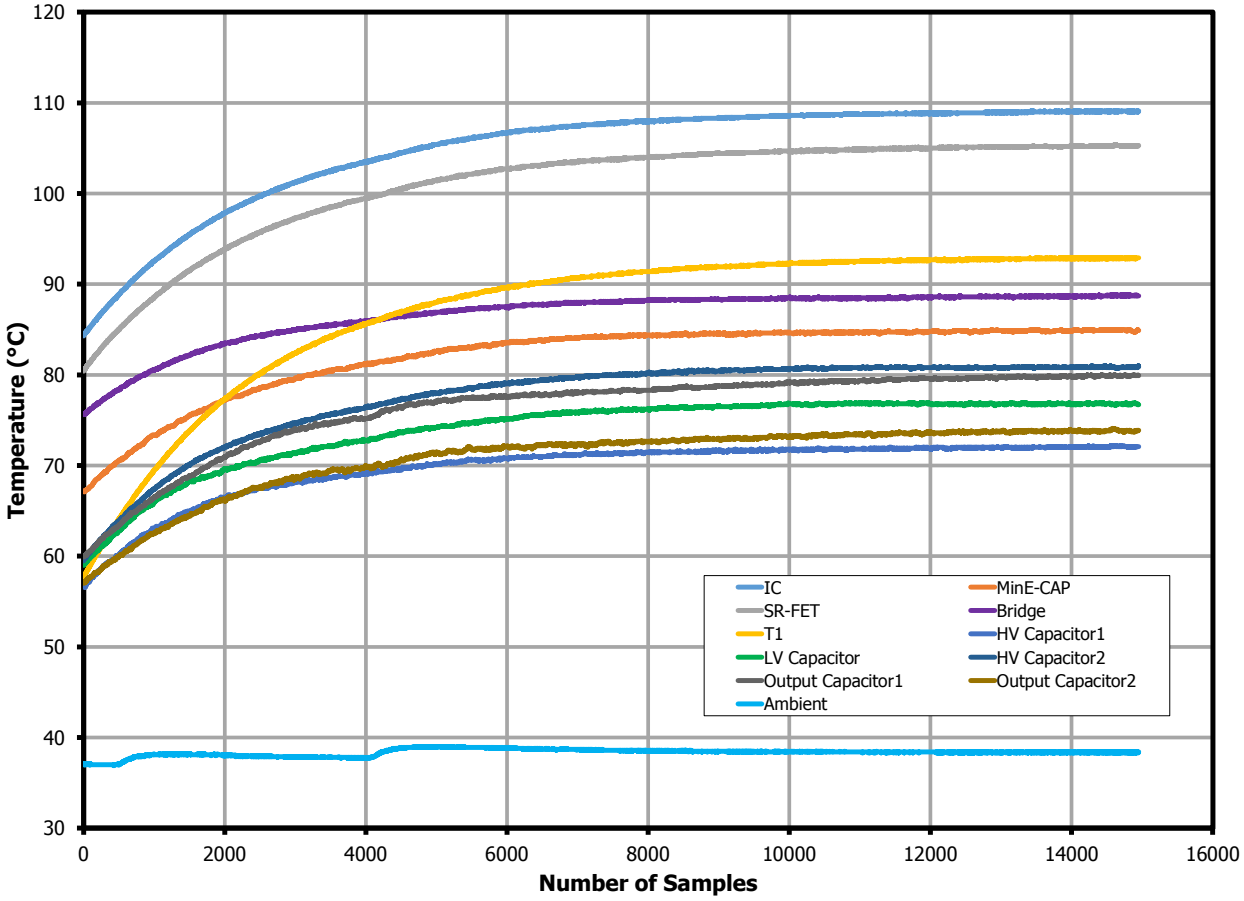

Figure 108 – Thermal Performance at 90 VAC, Full Load.

Component	Temperature (°C)
Ambient	39
INN3679C (U2)	109.1
MinE-CAP (U1)	85
SR FET (Q1)	105.4
Bridge (BR1)	88.8
Transformer (T1)	92.9
HV Capacitor1 (C2)	72.2
LV Capacitor (C3)	76.9
HV Capacitor2 (C5)	81
Output Capacitor1 (C18)	80
Output Capacitor2 (C19)	74.1

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12.3.2 265 VAC Full Load at 40 °C

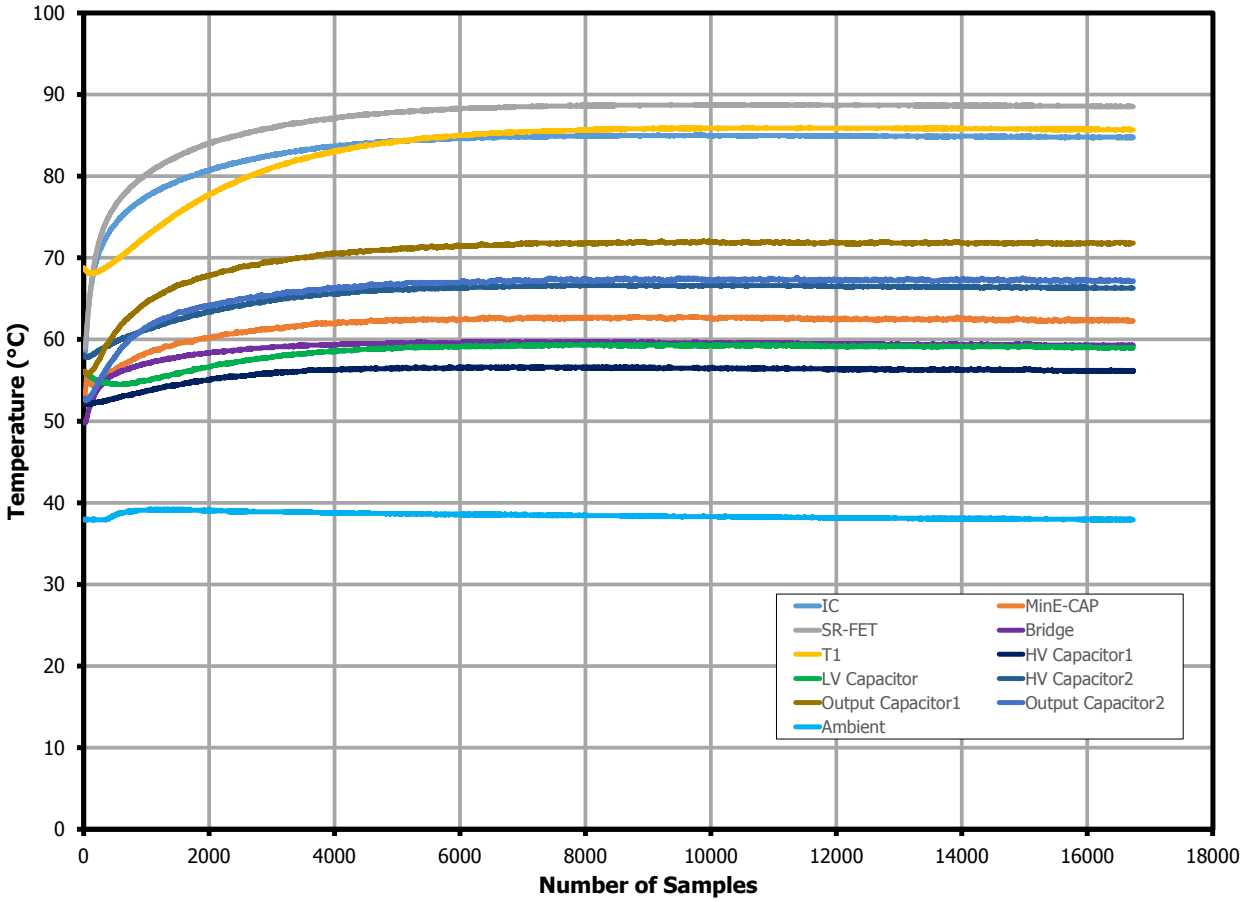

Figure 109 – Thermal Performance at 265 VAC, Full Load.

Component	Temperature (°C)
Ambient	39.2
INN3679C (U2)	85.1
MinE-CAP (U1)	62.8
SR FET (Q1)	88.8
Bridge (BR1)	59.7
Transformer (T1)	86
HV Capacitor1 (C2)	56.7
LV Capacitor (C3)	59.4
HV Capacitor2 (C5)	66.7
Output Capacitor1 (C18)	72.1
Output Capacitor2 (C19)	67.6

13 Conducted EMI

13.1 *115 VAC 3.25 A Resistive Load*

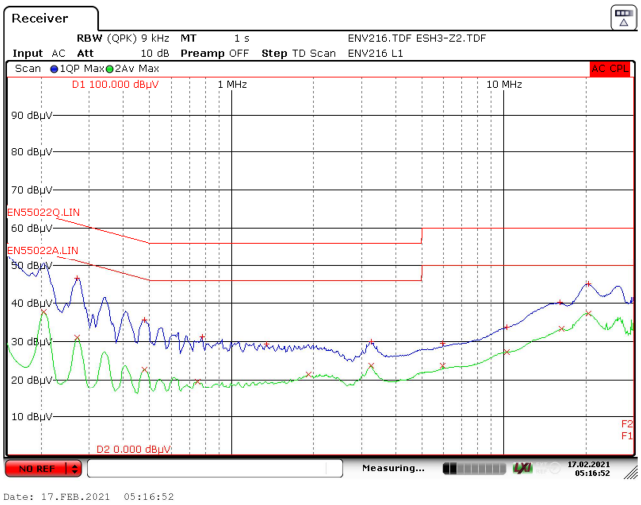

Figure 110 – Floating Output at 115 VAC: Line

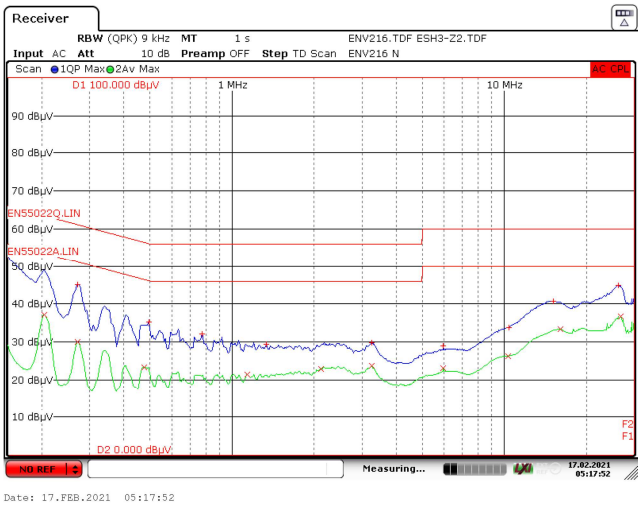

Figure 112 – Floating Output at 115 VAC: Neutral

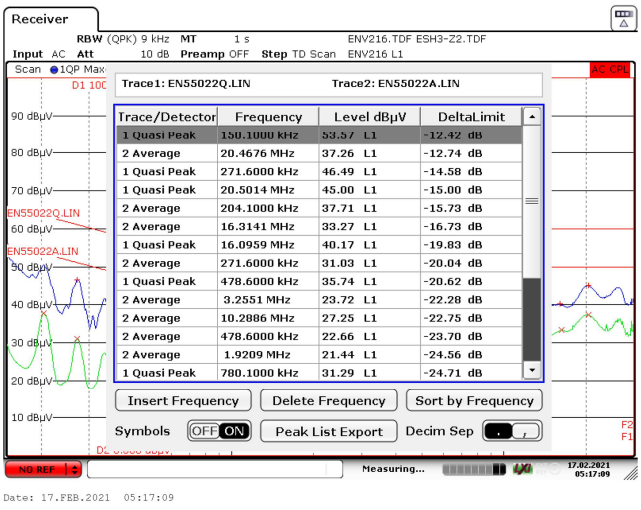

Figure 111 – Floating Output at 115 VAC: Peak Limits (Line)

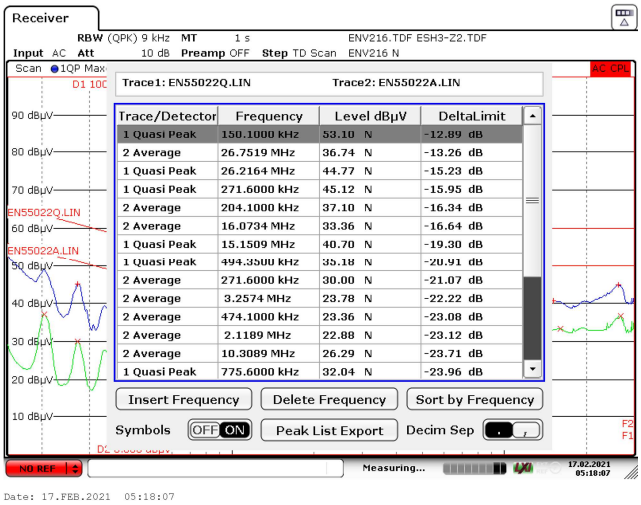

Figure 113 – Floating Output at 115 VAC: Peak Limits (Neutral)

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13.2 ***230 VAC 3.25 A Resistive Load***

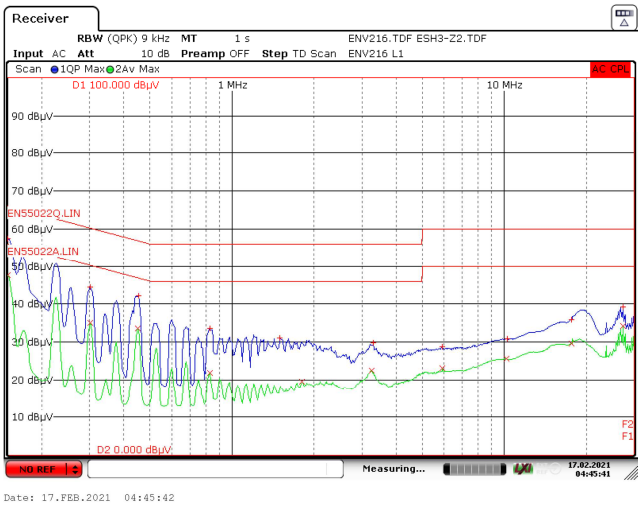

Figure 114 – Floating Output at 230 VAC: Line

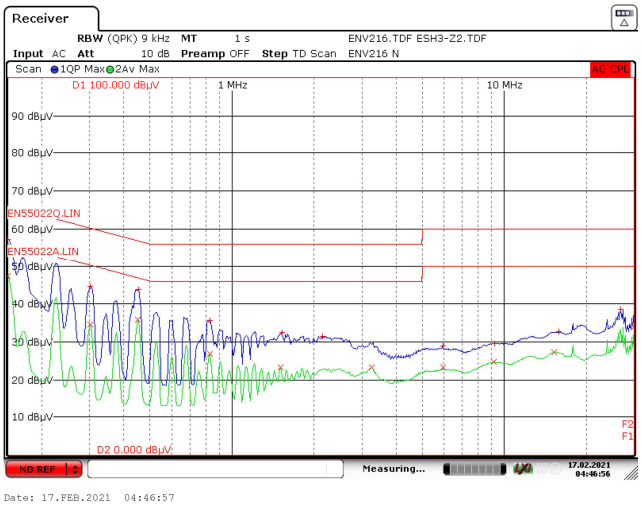

Figure 116 – Floating Output at 230 VAC: Neutral

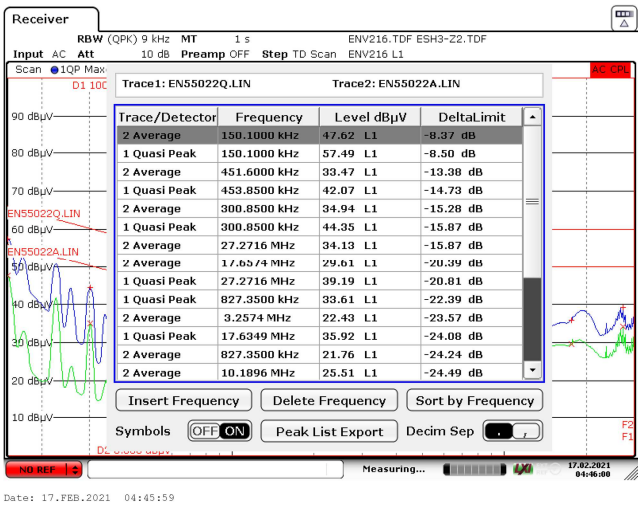

Figure 115 – Floating Output at 230 VAC: Peak Limits (Line)

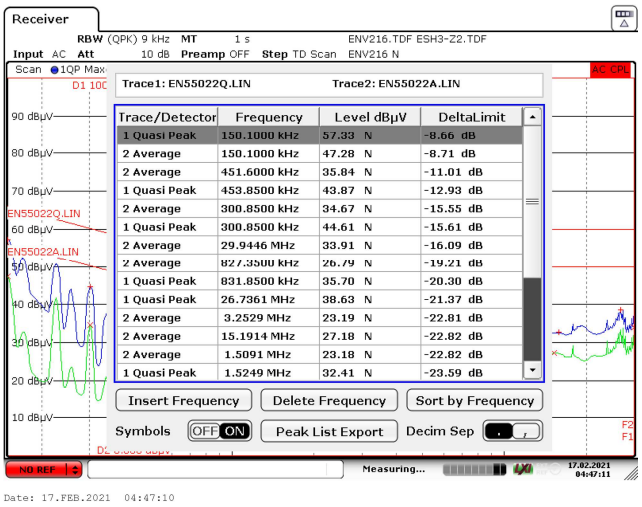

Figure 117 – Floating Output at 230 VAC: Peak Limits (Neutral)

14 Line Surge

Differential input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz.. Output was loaded at full load and operation was verified following each surge event.

14.1 *Differential Mode Surge*

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (º)	Test Result (Pass/Fail)
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+1000	230	L to N	180	Pass
-1000	230	L to N	180	Pass
+1000	230	L to N	270	Pass
-1000	230	L to N	270	Pass

14.1.1 1000 V 90º Differential Mode Surge

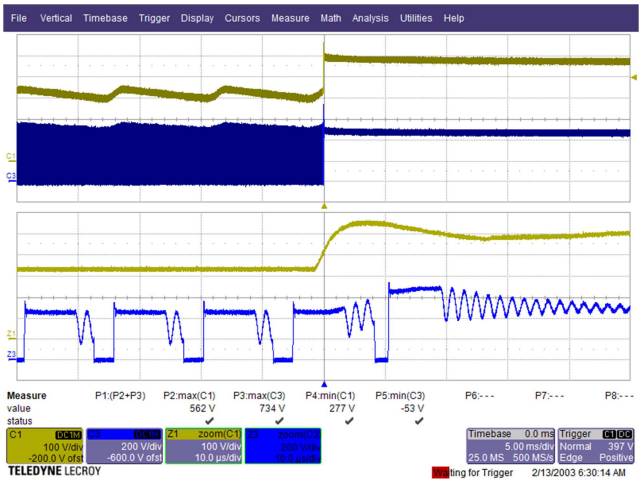

Figure 118 – Bulk Voltage and Drain Voltage, 230 VAC, Full Load.

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14.1.2 -1000 V 270º Differential Mode Surge

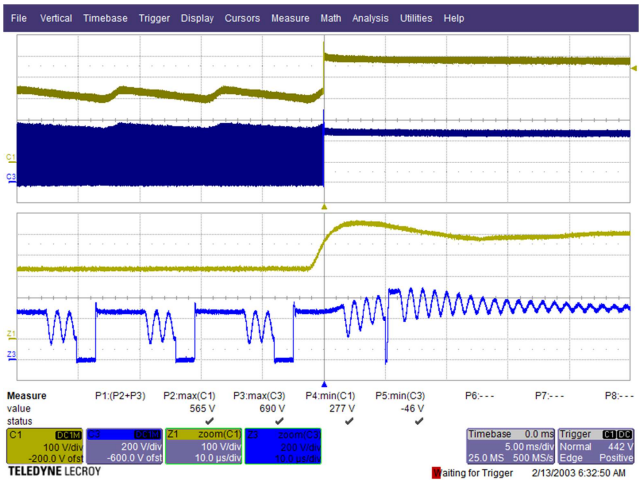

Figure 119 – Bulk Voltage and Drain Voltage, 230 VAC, Full Load.

15 **ESD**

Note: ESD performance was tested on limited number of units. All ESD strikes were applied at end of cable.

Passed ±8 kV contact discharge

Contact Voltage (kV)	Applied to	Number of Strikes	Test Result
+8	VOUT	10	Pass
	GND	10	Pass
-8	VOUT	10	Pass
	GND	10	Pass

Note: In all PASS results, no damage observed.

Passed ±15 kV Air discharge

Air Discharge Voltage (kV)	Applied to	Number of Strikes	Test Result
+15	VOUT	10	Pass
	GND	10	Pass
-15	VOUT	10	Pass
	GND	10	Pass

Note: In all PASS results, no damage was observed.

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16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
23-Mar-21	VRA/JD/TAC	1.0	Initial Release.	Apps & Mktg

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