Title	*Reference Design Report for a 12 W Dual Output Power Supply Using LinkSwitch-XT2SR LNK3773D*
Specification	90 VAC – 265 VAC Input; 5 V, 1.4 A and 12 V, 0.42 A Outputs
Application	Dual Output Open Frame Appliance Power Supply
Author	Applications Engineering Department
Document Number	RDR-962
Date	September 12, 2023
Revision	1.0

Summary and Features

- 12 W output from 90 VAC to 265 VAC
- Very low component count switcher solution with SR driver and integrated 3.3 V LDO (uVCC)
- Built-in synchronous rectification for >87% efficiency at nominal AC input
- <5 mW no-load input power at 230 VAC
- <200 mW standby input power at 5 V / 30 mA load
- Accurate thermal protection with hysteretic shutdown

PATENT INFORMATION
The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a 1.4 A, 5 V and 0.42 A, 12 V non-isolated dual output embedded power supply utilizing LNK3773D from the LinkSwitch-XT2SR family of ICs.

This design shows the high-power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

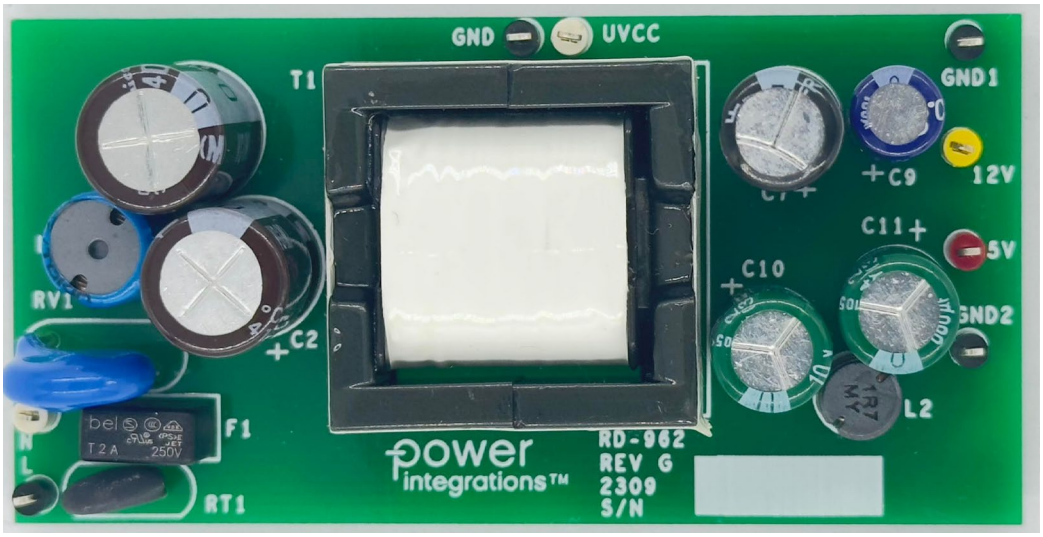


Figure 1 – Populated Circuit Board Photograph, Top.

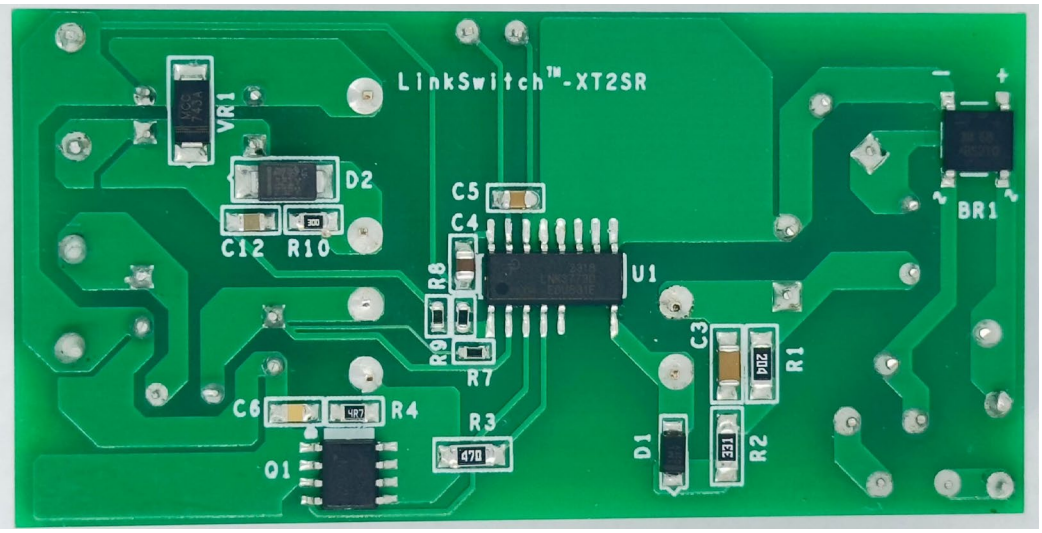


Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90	115/230	265	VAC	2 Wire Input.
Frequency	f_{LINE}		50/60		Hz	
No-Load Input Power			5		mW	
Standby Power (5 V / 30 mA)				200	mW	
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	±5 %
Output Ripple Voltage 1	$V_{RIPPLE1}$		50		mV	Measured at Full load, 20 MHz Bandwidth.
Output Current 1	I_{OUT1}	0	1.4		A	
Output Voltage 2	V_{OUT2}	10.2	12	13.8	V	±15 %, (±10 % with 10% Min Load on 12 V.)
Output Ripple Voltage 2	$V_{RIPPLE2}$		120		mV	Measured at Full load, 20 MHz Bandwidth.
Output Current 2	I_{OUT2}	0	0.42		A	
uVCC Voltage	V_{uVCC}		3.3		V	
uVCC Current	I_{uVCC}			20	mA	
Total Output Power						
Continuous Output Power	P_{OUT}			12	W	
Efficiency						
Average	$\eta_{AVE[BRD]}$	87			%	Measured at 115 / 230 VAC, P_{OUT} 25 ºC.
25%, 50%, 75%, and 100%						V_{IN} at 230 VAC.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B Load Floating				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge						
Differential		1			kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω.
Common mode Ring Wave		6			kV	100 kHz Ring Wave, 12 Ω Common Mode.
EFT		2			kV	5 kHz, 15 ms burst time, 120s repetition time, 12 Ω EFT 100 kHz, 750 µs burst time, 120s repetition time, 12 Ω EFT
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.

3 Schematic

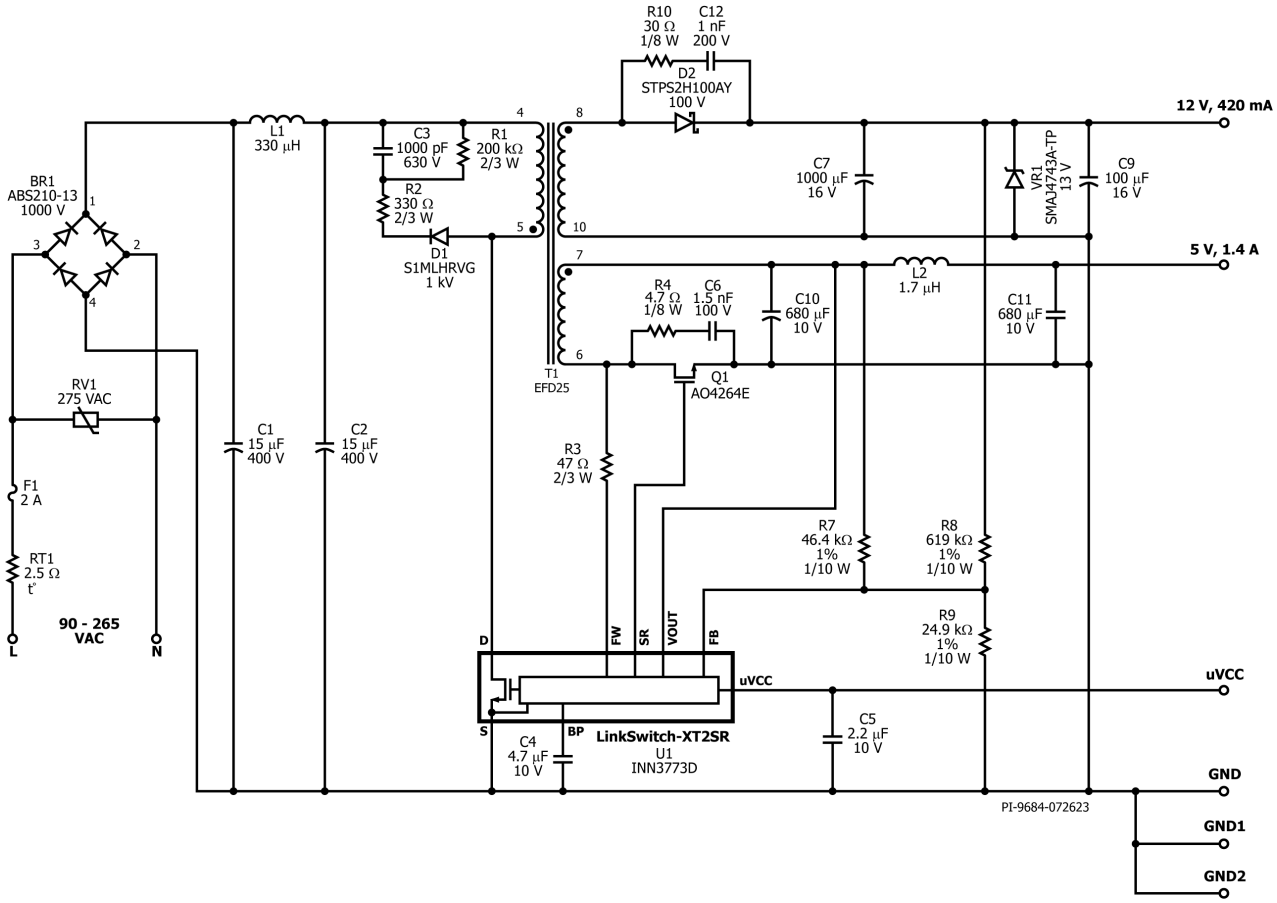


Figure 3 – Schematic.

4 Circuit Description

This circuit is a non-isolated dual output flyback power supply for appliances using the LinkSwitch-XT2SR IC (U1). Using the optional external feedback pin for the dual output design, features a highly efficient design satisfying cross regulation requirements without a post regulator. This circuit makes use of the synchronous rectifier for 5 V output to improve efficiency.

4.1 *Input EMI Filtering*

Input Fuse F1 isolates the circuit and provides protection against excess input current resulting from catastrophic failure of any of the components in the power supply.

Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply.

Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter consisting of capacitors C1 and C2. The differential inductance of L1 is connected between C1 and C2, forms a pi-filter to attenuate differential mode EMI.

4.2 *LinkSwitch-XT2SR Primary-Side Circuit*

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the integrated 725 V power MOSFET inside the LinkSwitch-XT2SR IC (U1)

A low-cost R2CD clamp circuit formed by D1, R1, R2, and C3 limits the peak drain voltage at the instant of turn-off of the switch inside U1. The clamp circuit helps to dissipate the energy stored in the leakage inductance of transformer T1 and output traces.

The LinkSwitch-XT2SR IC is self-starting, using an internal high-voltage current source to charge the BP pin capacitor, C4 when AC is first applied. During normal operation the BP regulator is powered from VOUT. The minimum drain voltage at startup before the IC starts switching is 50 VDC, and VOUT will be used to charge BP when VOUT voltage reaches 0.2 V higher than BP voltage.

4.3 *LinkSwitch-XT2SR Secondary-Side Circuit*

The controller of the LinkSwitch-XT2SR IC provides output voltage sensing and drives to a switch providing synchronous rectification.

The 5 V output of the transformer is rectified by SR FET Q1. Very low ESR capacitors C10 and C11 with L2, provide filtering and significantly attenuates high frequency ripple and noise at the 5 V output. RC snubber network comprising of R4 and C6 damp high frequency ringing across the SR FET during switching transients that would otherwise create radiated EMI.

The 12 V output of the transformer is rectified by Schottky diode D2. Low ESR capacitor C7 and ceramic capacitor C9, provides filtering and significantly attenuates the high frequency ripple and noise at 12 V output. RC snubber network comprising of R10 and C12 damp high frequency ringing across the Schottky Diode during switching transients that would otherwise create radiated EMI.

Synchronous rectification (SR) is provided by switch Q1. Switch Q1 is turned on by the controller inside IC U1, based on the winding voltage sensed via resistor R3 and current fed into FORWARD pin of the IC.

In continuous conduction mode operation, the SR FET is turned off just prior to the controller commanding a new switching cycle. In discontinuous mode the SR FET is turned off when the voltage drop across the MOSFET falls below a threshold ($V_{SR(TH)}$). The controller ensures that it is never on simultaneously with the synchronous rectification MOSFET.

Resistor R7, R8 and R9 form an external voltage divider network that senses the output voltage from both outputs for better cross-regulation. Zener diode VR1 improves the cross regulation when only the 5 V output is loaded, which results in the 12 V output operating at the higher end of the specification. The LinkSwitch-XT2SR IC has an internal reference of 2.0 V, and the unit enters auto-restart when the VOUT pin voltage goes up higher than 6 V.

There is a 3.3 V uVCC output with C5 decoupling capacitor, which can deliver up to 20 mA maximum current.

5 PCB Layout

Layers: One (1)
Board Material: FR4
Board Thickness: 0.062”
Copper Weight: 2 oz (2.8 mils / 71 μm) unless otherwise stated.

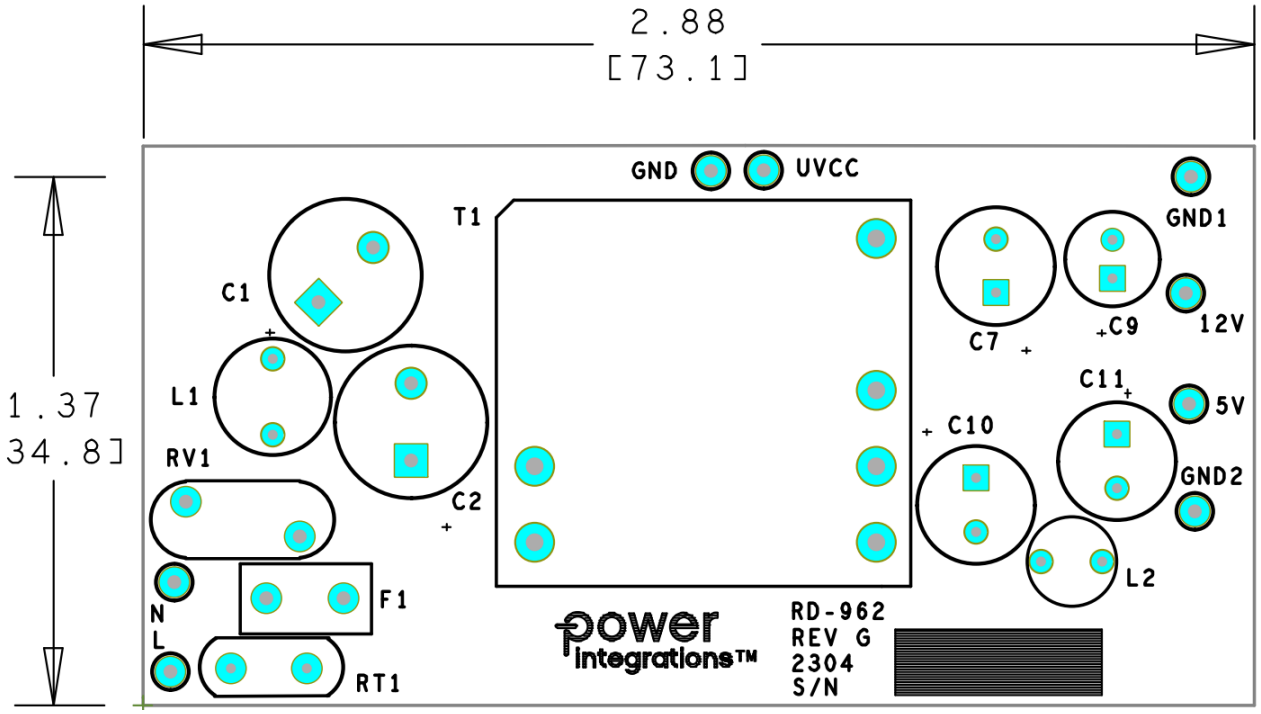


Figure 4 – Printed Circuit Layout, Top.

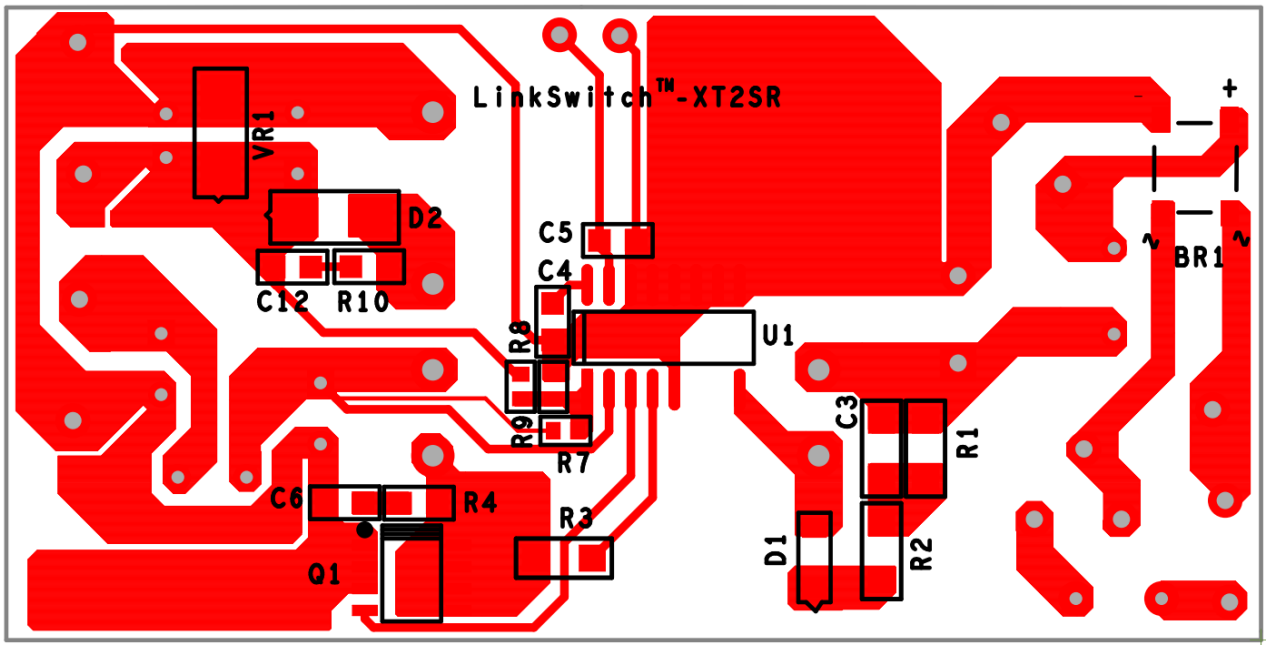


Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 2 A, Bridge Rectifier, SMD, 4SOPA	ABS210-13	Diodes, Inc.
2	2	C1 C2	15 μF, ±20%, 400 V, Electrolytic Capacitor, (10 x 16)	UVC2G150MPD	Nichicon
3	1	C3	1000 pF, ±10%, 630 V, Ceramic Capacitor, X7R, 1206	C1206C102KBRACTU	Kemet
4	1	C4	4.7 μF, ±10%, 10 V, Ceramic Capacitor, X7R 0805	LMK212B7475KGHT	Taiyo Yuden
5	1	C5	2.2 μF, ±20%, 10 V, Ceramic Capacitor, X7R, 0805	C0805C225M8RACTU	Kemet
6	1	C6	1.5 nF, ±10%, 100 V, Ceramic Capacitor, X7R, 0805	CC0805KRX7R9BB152	Yageo
7	1	C7	1000 μF, ±20%, 16 V, Electrolytic Capacitor, Low ESR, (8 x 20)	EEU-FR1C102LB	Panasonic
8	1	C9	100 μF, ±20%, 16 V, Electrolytic Capacitor, Low ESR, 250 mΩ, (6.3 x 13)	ELXZ160ELL101MFB5D	Nippon Chemi-Con
9	2	C10 C11	680 μF, ±20%, 10 V, Electrolytic Capacitor, Very Low ESR, 56 mΩ, (8 x 15)	EKZE100ELL681MH15D	Nippon Chemi-Con
10	1	C12	1 nF, 10%, 200 V, Ceramic Capacitor, X7R, 0805	08052C102KAT2A	AVX
11	1	D1	1000 V, 1 A, Diode, General Purpose, SMT, SUB SMA	S1MLHRVG	Taiwan Semi
12	1	D2	100 V, 2 A, Diode, Schottky, SMT, SMA (DO-214AC)	STPS2H100AY	ST Micro
13	1	F1	2 A, 250 V, Fuse, Slow, Long Time Lag, RST	RST 2	Belfuse
14	1	L1	330 μH, Unshielded Drum Core, Wirewound Inductor, 0.55 A, 720 mΩ Max, Radial 9 x 11.5 mm	SBC3-331-551	Tokin
15	1	L2	1.7 μH, Unshielded Drum Core, Wirewound, Inductor, 3.52A, 22.8 mΩ Max, Radial, 6 x 6.5 mm	RCH664NP-1R7M	Sumida
16	1	Q1	N-Channel, 60 V, 13.5A (Ta), 3.1W (Ta), SMT, 8-SO, 8-SOP, PG-DSO-8, 8-SOIC (0.154", 3.90 mm Width)	AO4264E	Alpha & Omega Semi
17	1	R1	RES, 200 kΩ, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J204V	Panasonic
18	1	R2	RES, 330 Ω, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J331V	Panasonic
19	1	R3	RES, 47 Ω, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J470V	Panasonic
20	1	R4	RES, 4.7 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ4R7V	Panasonic
21	1	R7	RES, 46.4 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF4642V	Panasonic
22	1	R8	RES, 619 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF6193V	Panasonic
23	1	R9	RES, 24.9 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2492V	Panasonic
24	1	R10	RES, 30 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ300V	Panasonic
25	1	RT1	NTC Thermistor, 2.5 Ω, 3 A	SL08 2R503	Ametherm
26	1	RV1	275 Vac, 43 J, 10 mm, Radial	S10K275	Epcos
27	1	T1	Bobbin, EFD25, Horizontal, 10 pins Transformer	B66422-B1010-D1 PNK-37730	Epcos Premier Magnetics
28	1	U1	LinkSwitch-XT2SR, SO-16B, High voltage	LNK3773D	Power Integrations
29	1	VR1	13 V, 1 W, ±5%, Zener Diode, SMT, DO-214AC (SMA)	SMAJ4743A-TP	Micro Commercial
30	1	12V	Test Point, YELLOW, PC MINI, 0.040" (1.02 mm) Dia, TH MOUNT	5004	Keystone
31	1	5V	Test Point, RED, Miniature TH MOUNT	5000	Keystone
32	4	GND GND1 GND2 L	Test Point, BLK, Miniature TH MOUNT	5001	Keystone
33	2	N UVCC	Test Point, WHT, Miniature TH MOUNT	5002	Keystone

7 Transformer (T1) Specification

7.1 *Electrical Diagram*

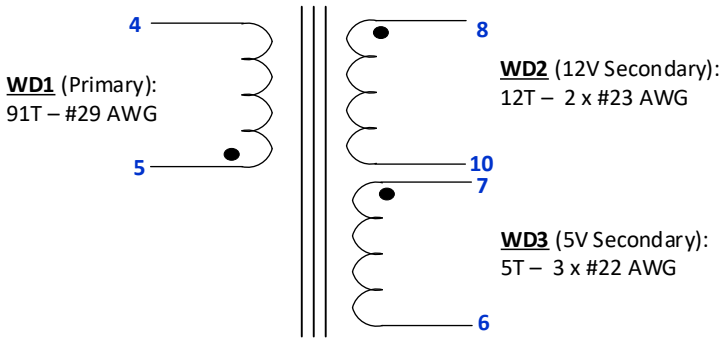


Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 4 and 5, with all other windings open.	2366 µH ±10%
Primary Leakage Inductance	Between pin 4 and 5, with all secondary pins: 6, 7, 8 & 10 shorted.	16 µH (Max).

7.3 *Material List*

Item	Description
[1]	Core: EFD25, N87 or equivalent, Gapped
[2]	Bobbin: EFD25-H-10-Pins. YingChin.
[3]	Magnet Wire: #29 AWG, Double Coated.
[4]	Magnet Wire: #23 AWG, Double Coated.
[5]	Magnet Wire: #22 AWG, Triple Insulated Wire.
[6]	Barrier Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 16.7 mm Width.
[7]	Barrier Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 8.0 mm Width.
[8]	Varnish: Dolph BC-359.

7.4 *Transformer Build Diagram*

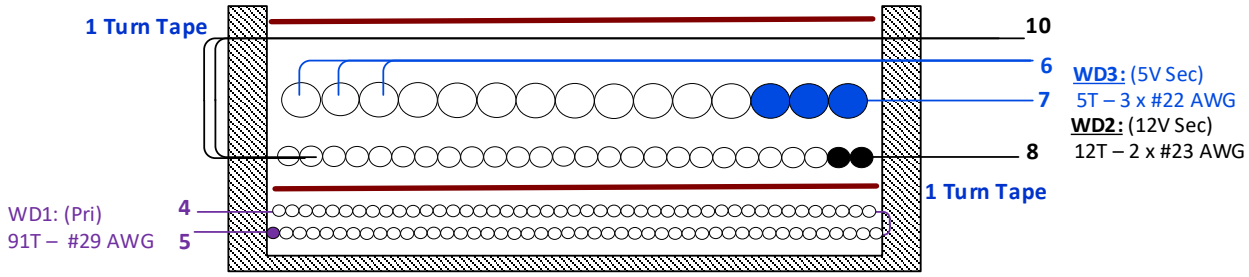
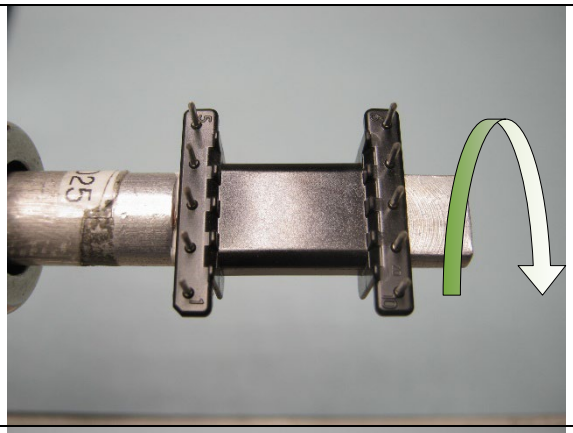
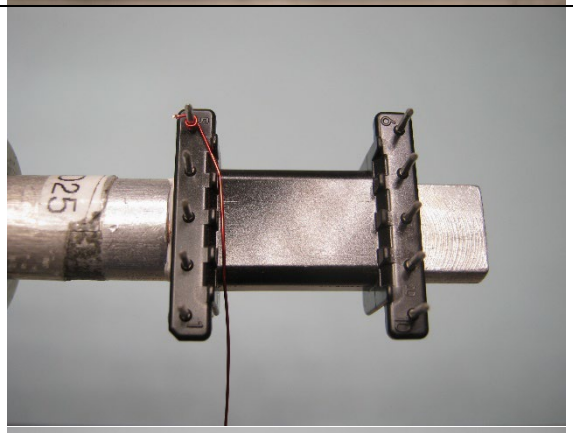
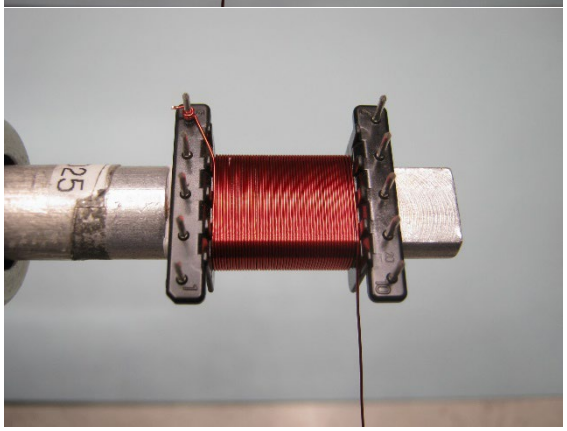


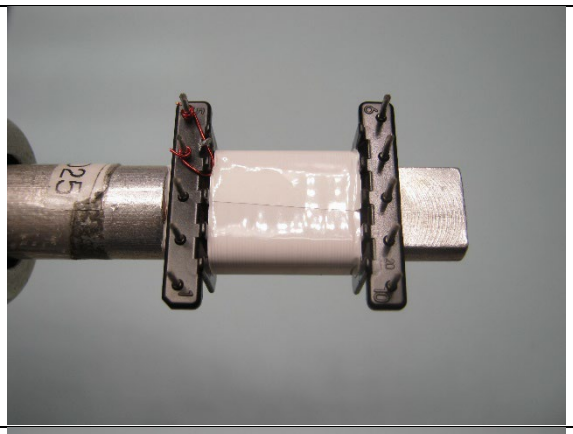
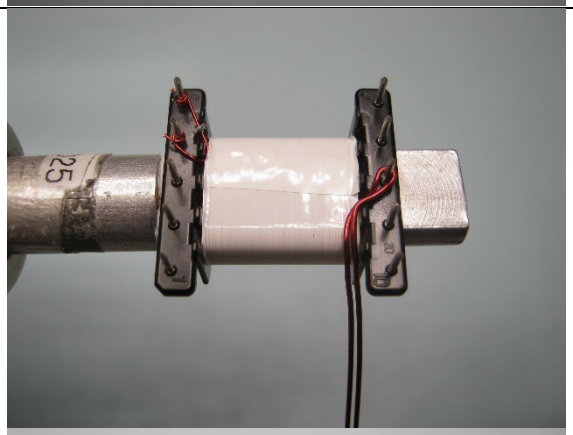
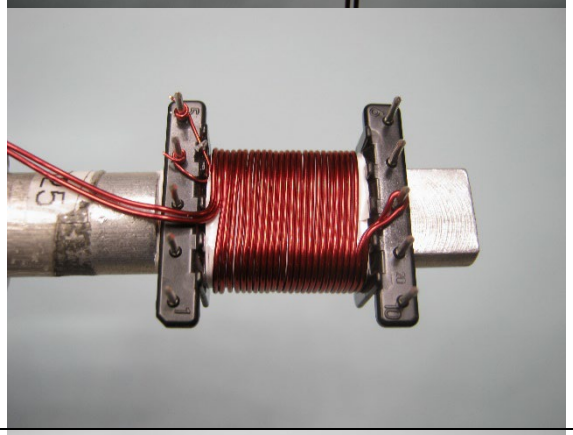
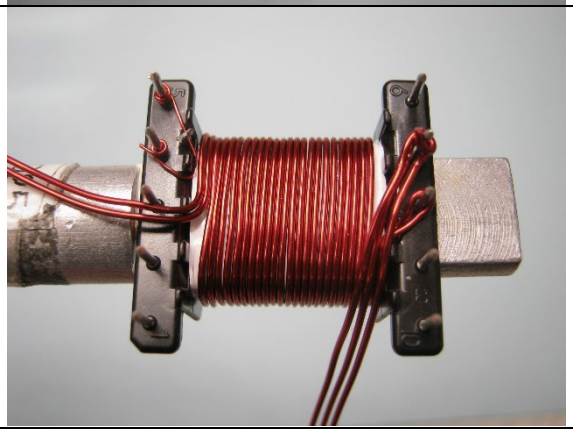
Figure 7 – Transformer Electrical Diagram.

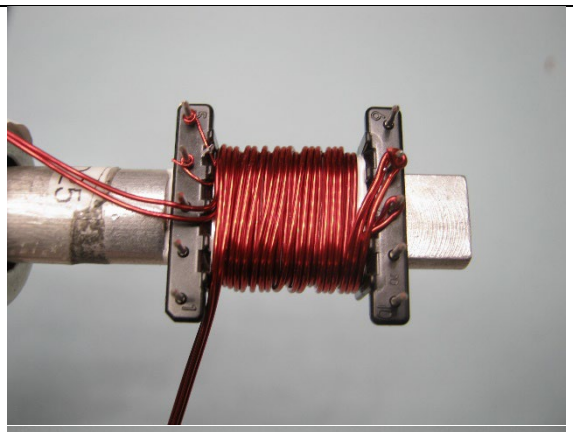
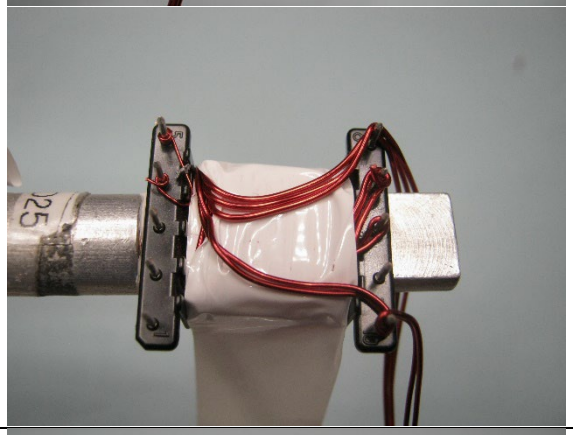
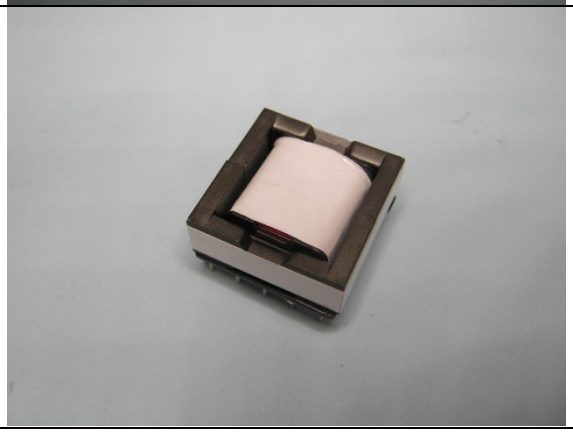
7.5 *Winding Instructions*

Winding Preparation	Position the bobbin Item [2] on the mandrel such that the primary-side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
WD1 Primary	Start at pin 5, wind 48 turns of wire Item [3] in 1st layer, with tight tension, from left to right. Then continue to wind from right to left 43 turns on second layer, spread the wire evenly. At the last turn, terminate the wire at pin 4.
Insulation	1 layer of tape Item [6].
WD2 12 V - Secondary	Start from pin 8, use 2 wires Item [4], wind 12 bifilar turns from right to left. At the last turn, leave wire floating ~1" long for later termination.
WD3 5 V - Secondary	Start at pin 7, use 3 wires Item [5], wind 5 tri-filar turns from right to left. At the last turn, place tape Item [6] to hold the wires of this winding, then bring wires back to the right to terminate at pin 6. Also, by this time, bring 2 wires of WD2 floating to the left and terminate at pin 10.
Insulation	2 layer of tape Item [6] to secures all windings
Finish	Gap core halves to get 2366 μH and secure with tape item [7]. Varnish with Item [8].

7.6 *Winding Illustrations*

Winding Preparation		Position the bobbin Item [2] on the mandrel such that the primary-side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
WD1 **Primary**	 	Start at pin 5, wind 48 turns of wire Item [3] on 1st layer, with tight tension, from left to right. Then continue to wind from right to left 43 turns on second layer, spread the wire evenly. At the last turn, terminate the wire at pin 4.

Insulation		1 layer of tape Item [6].
WD2 **12V- Secondary**	 	Start from pin 8, use 2 wires Item [4], wind 12 bifilar turns from right to left. At the last turn, leave wire floating ~1" long for later termination.
WD3 **5V- Secondary**		Start at pin 7, use 3 wires Item [5], wind 5 tri-filar turns from right to left. At the last turn, place tape Item [6] to hold the wires of this winding, then bring wires back to the right to terminate at pin 6. Also, by this time, bring 2 wires of WD2 floating to the left and terminate at pin 10.

	 	
Insulation		2 layer of tape Item [6] to secures all windings
Finish		Gap core halves to get 2366 μH and secure with tape Item [7]. Varnish with Item [8].

7.7 *Transformer Design Spreadsheet*

ACDC_LinkSwitchXT2SR_Flyback_081623; Rev.1.1; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNIT	ACDC LinkSwitch-XT2SR Flyback Design Spreadsheet
APPLICATION VARIABLES					
LINE VOLTAGE RANGE			UNIVERSAL		AC line voltage range
VACMIN			90.00	V	Minimum AC line voltage
VACMAX			265.00	V	Maximum AC line voltage
fL			60.00	Hz	AC mains frequency
LINE RECTIFICATION TYPE	F		F		Line rectification type: select "F" if full wave rectification or "H" if half wave rectification
VOUT			5.00	V	Output voltage
IOUT	2.400		2.400	A	Average output current
EFFICIENCY (User Estimate)			0.80		Overall efficiency estimate
LOSS ALLOCATION FACTOR			0.50		The ratio of power losses during the primary switch off-state to the total system losses
POUT			12.00	W	Continuous output power
CIN	30.00		30.00	uF	Input capacitor
VMIN			99.77	V	Valley voltage of the rectified minimum AC line voltage
VMAX			374.77	V	Peak voltage of the maximum AC line voltage
FEEDBACK	EXTERNAL		EXTERNAL		Feedback type: select either "INTERNAL" or "EXTERNAL"
INPUT STAGE RESISTANCE			10.0	Ohms	Input stage resistance (includes thermistor, filtering components, etc)
PLOSS_INPUTSTAGE			0.226	W	Maximum input stage power loss
LINKSWITCH-XT2 VARIABLES					
DEVICE SERIES	LNK3773D		LNK3773D		Generic LinkSwitch-XT2SR device code
POUT_MAX			12	W	Power capability of the device based on thermal performance
ILIMITMIN			0.478	A	Minimum current limit of the device
ILIMITTYP			0.514	A	Typical current limit of the device
ILIMITMAX			0.550	A	Maximum current limit of the device
RDSON			6.85	Ohms	Switch on-state drain-to-source resistance at 100 degC
FSMIN			62000	Hz	Minimum switching frequency
FSTYP			66000	Hz	Typical switching frequency
FSMAX			70000	Hz	Maximum switching frequency
BVDSS			725	V	Device breakdown voltage
PRIMARY WAVEFORM PARAMETERS					
OPERATION MODE			CCM		Continuous mode of operation
VOR	92.0		92.0	V	Voltage reflected across the primary winding when the primary switch is off
VDSON			2.00	V	Primary switch on-time drain-to-source voltage
VDSOFF			536.8	V	Primary switch off-time drain-to-source voltage stress
KRP/KDP			0.676		Degree on how much the operation tend to be continuous or discontinuous
KP_TRANSIENT			0.312		KP value under transient conditions
DUTY			0.485		Maximum duty cycle
TIME_ON_MIN			2.731	us	Primary switch minimum on-time
IPEAK_PRIMARY			0.550	A	Maximum primary peak current
IPED_PRIMARY			0.155	A	Maximum primary pedestal current
IAVG_PRIMARY			0.153	A	Maximum primary average current
IRMS_PRIMARY			0.240	A	Maximum root-mean-squared value of the primary current

PLOSS_SWITCH			0.512	W	Maximum primary switch power loss
THERMAL RESISTANCE OF SWITCH			95	degC/W	Net thermal resistance of primary switch
T_RISE_SWITCH			48.6	degC	Maximum temperature rise of the switch in degrees Celsius
LPRIMARY_MIN			2130	uH	Minimum primary inductance
LPRIMARY_TYP			2366	uH	Typical primary inductance
LPRIMARY_MAX			2603	uH	Maximum primary inductance
LPRIMARY_TOL			10	%	Primary inductance tolerance
SECONDARY WAVEFORM PARAMETERS					
IPEAK_SECONDARY			10.010	A	Peak secondary current
IRMS_SECONDARY			4.494	A	Maximum root-mean-squared value of the secondary current
IRIPPLE_SECONDARY			10.010	A	Maximum ripple value of the secondary current
PIV_SECONDARY			25.5	V	Peak inverse voltage of the secondary rectifier
VF_SECONDARY	0.10		0.10	V	Forward voltage drop of the secondary rectifier
TRANSFORMER CONSTRUCTION PARAMETERS					
CORE	CUSTOM		CUSTOM		Select the transformer core
CODE CODE	EFD25		EFD25		Core code
BOBBIN	EFD25-H		EFD25-H		Core code
AE	58.00		58.00	mm^2	Cross-sectional area of the core
LE	57.00		57.00	mm	Effective magnetic path length of the core
AL	2000.0		2000.0	nH/(T^2)	Ungapped effective inductance of the core
VE	3300.0		3300.0	mm^3	Effective volume of the core
AW	40.70		40.70	mm^2	Window area of the bobbin
BW	16.10		16.10	mm	Width of the bobbin
MLT	50.00		50.00	mm	Mean length per turn of the bobbin
MARGIN			0.00	mm	Safety margin
CORE	CUSTOM		CUSTOM		Select the transformer core
NPRIMARY			91	turns	Primary winding number of turns
BMAX			2712	Gauss	Actual value of magnetic flux density (BMAX_TARGET = 3000 Gauss)
BAC			1356	Gauss	AC flux density
ALG			286	nH/(T^2)	Gapped core effective inductance
LG			0.219	mm	Core gap length
NPRIMARY			91	turns	Primary winding number of turns
BMAX			2712	Gauss	Actual value of magnetic flux density (BMAX_TARGET = 3000 Gauss)
Secondary Winding					
NSECONDARY	5		5	turns	Secondary winding number of turns
FEEDBACK PARAMETERS					
VFBRATIO			0.80		Output voltage feedback priority ratio. Eg. Ratio of 0.8 implies that VOUT1 has an 80% feedback priority.
RUPPER1			46400	Ohms	FB pin upper resistor connected to VOUT1
RUPPER2			619000	Ohms	FB pin upper resistor connected to VOUT2
RLOWER	24900		24900	Ohms	FB pin (Lower) Resistor
VFBRATIO			0.80		Output voltage feedback priority ratio. Eg. Ratio of 0.8 implies that VOUT1 has an 80% feedback priority.
MULTIPLE OUTPUT PARAMETERS					
Output 1 (SRFET)					
VOUT1			5.00	V	Output voltage 1
IOUT1	1.400		1.400	A	Output current 1
POUT1			7.00	W	Output power 1
VD1	0.10		0.10	V	Forward voltage drop of SRFET for output 1
NS1			5	turns	Number of turns for output 1

ISPEAK1			10.01	A	Instantaneous peak value of the secondary current for output 1
ISRMS1			2.621	A	Root-mean-squared value of the secondary current for output 1
ISRIPPLE1			10.010	A	Current ripple on the secondary current waveform for output 1
PIV1			31.9	V	Computed peak inverse voltage stress on the secondary SRFET for output 1
OUTPUT_RECTIFIER1	AO4264E		AO4264E		Selected SRFET for output 1
VRRM1			60	V	Maximum repetitive peak reverse voltage of the output rectifier for output 1
TRR1			19	ns	Reverse recovery time of the output rectifier for output 1
IFM1			13.50	A	Maximum forward continuous current of the output rectifier for output 1
PLOSS_DIODE1			0.512	W	Maximum secondary diode power loss for output 1
VOUT1_RIPPLE			50	mV	Output voltage ripple for output 1
ESR_COUT1			5	mOhms	Equivalent series resistance of the output capacitor for output 1
IRMS_COUT1			2.216	A	Root-mean-squared value of the output capacitor current for output 1
PLOSS_COUT1			0.025	W	Maximum output capacitor power loss for output 1
Output 2 (Diode)					
VOUT2	12.00		12.00	V	Output voltage 2
IOUT2	0.420		0.420	A	Output current 2
POUT2			5.04	W	Output power 2
VD2	0.20		0.20	V	Forward voltage drop of diode for output 2
NS2			12	turns	Number of turns for output 2
ISPEAK2			4.171	A	Instantaneous peak value of the secondary current for output 2
ISRMS2			0.786	A	Root-mean-squared value of the secondary current for output 2
ISRIPPLE2			4.171	A	Current ripple on the secondary current waveform for output 2
PIV2_CALCULATED			83.8	V	Computed peak inverse voltage stress on the diode for output 2
OUTPUT_RECTIFIER2	STPS2H100AY		STPS2H100AY		Selected diode for output 2
PIV2_RATING			100	V	Peak inverse voltage rating on the diode for output 2
TRR2			0	ns	Reverse recovery time of the diode for output 2
IFM2			2.00	A	Maximum forward continuous current of the diode for output 2
PLOSS_DIODE2			0.064	W	Maximum diode power loss for output 2
VOUT2_RIPPLE			120	mV	Output voltage ripple for output 2
ESR_COUT2			29	mOhms	Equivalent series resistance of the output capacitor for output 2
IRMS_COUT2			0.665	A	Root-mean-squared value of the output capacitor current for output 2
PLOSS_COUT2			0.013	W	Maximum output capacitor power loss for output 2
POUT_TOTAL			12.04	W	The total power of all outputs.
NEGATIVE OUTPUT	N/A		N/A		If a negative output exists, select the output number (e.g. if VO2 is a negative output, select 2)

8 Performance Data

8.1 *Average Efficiency*

Note: Measured across PCB output terminals.

Requirement	
Average	**74.74% (DOE6) 80.3% (CoC II)**
10%	**71% (CoC II)**

8.1.1 115 VAC Input (uVCC = 3.3 V / 0 A)

% Load	P_{IN} (W)	$5V_{OUT}$ (V_{DC})	$5I_{OUT}$ (A_{DC})	$5P_{OUT}$ (W)	$12V_{OUT}$ (V_{DC})	$12I_{OUT}$ (A_{DC})	$12P_{OUT}$ (W)	$P_{OUT-Total}$ (W)	Efficiency (%)	Average Efficiency (%)
100%	13.46	4.92	1.40	6.89	11.64	0.42	4.88	11.77	87.44	
75%	10.16	4.99	1.05	5.24	11.76	0.315	3.70	8.94	87.99	
50%	6.76	5.00	0.7	3.49	11.75	0.210	2.46	5.95	88.01	
25%	3.39	5.00	0.35	1.74	11.74	0.105	1.23	2.97	87.61	**87.77**
10%	1.38	5.00	0.14	0.69	11.73	0.042	0.49	1.18	**85.51**	

8.1.2 230 VAC Input (uVCC = 3.3 V / 0 A)

% Load	P_{IN} (W)	$5V_{OUT}$ (V_{DC})	$5I_{OUT}$ (A_{DC})	$5P_{OUT}$ (W)	$12V_{OUT}$ (V_{DC})	$12I_{OUT}$ (A_{DC})	$12P_{OUT}$ (W)	$P_{OUT-Total}$ (W)	Efficiency (%)	Average Efficiency (%)
100%	13.45	4.93	1.40	6.91	11.65	0.42	4.89	11.8	87.73	
75%	10.16	4.99	1.05	5.24	11.78	0.315	3.71	8.95	88.09	
50%	6.80	5.00	0.7	3.49	11.74	0.210	2.46	5.95	87.5	
25%	3.45	5.00	0.35	1.74	11.72	0.105	1.23	2.97	86.09	**87.35**
10%	1.40	5.00	0.14	0.69	11.73	0.042	0.49	1.18	**84.28**	

8.1.3 115 VAC Input (uVCC = 3.3 V / 20 mA)

% Load	P_{IN} (W)	$5V_{OUT}$ (V_{DC})	$5I_{OUT}$ (A_{DC})	$5P_{OUT}$ (W)	$12V_{OUT}$ (V_{DC})	$12I_{OUT}$ (A_{DC})	$12P_{OUT}$ (W)	$3.3V_{OUT}$ (V_{DC})	$3.3P_{OUT}$ (W)	$P_{OUT-Total}$ (W)	Eff (%)	Average Efficiency (%)
100%	13.58	4.92	1.40	6.89	11.65	0.42	4.89	3.24	0.069	11.85	87.25	
75%	10.27	4.99	1.05	5.23	11.76	0.315	3.70	3.24	0.069	9.00	87.62	
50%	6.84	5.00	0.7	3.49	11.76	0.210	2.46	3.24	0.069	6.02	88.00	
25%	3.51	5.00	0.35	1.74	11.75	0.105	1.23	3.24	0.069	3.04	86.58	**87.36**
10%	1.504	5.00	0.14	0.69	11.78	0.042	0.49	3.24	0.069	1.25	**83.05**	

8.1.4 230 VAC Input (uVCC = 3.3 V / 20 mA)

% Load	P_{IN} (W)	$5V_{OUT}$ (V_{DC})	$5I_{OUT}$ (A_{DC})	$5P_{OUT}$ (W)	$12V_{OUT}$ (V_{DC})	$12I_{OUT}$ (A_{DC})	$12P_{OUT}$ (W)	$3.3V_{OUT}$ (V_{DC})	$3.3P_{OUT}$ (W)	$P_{OUT-Total}$ (W)	Eff (%)	Average Efficiency (%)
100%	13.57	4.93	1.40	6.91	11.66	0.42	4.89	3.24	0.069	11.87	87.46	
75%	10.26	4.99	1.05	5.24	11.78	0.315	3.70	3.24	0.069	9.01	87.81	
50%	6.91	5.00	0.7	3.49	11.77	0.210	2.47	3.24	0.069	6.03	87.25	
25%	3.57	5.00	0.35	1.74	11.75	0.105	1.23	3.24	0.069	3.04	85.13	**86.91**
10%	1.53	5.00	0.14	0.69	11.78	0.042	0.49	3.24	0.069	1.25	**81.63**	

8.2 *Full Load Efficiency vs. Line*

Note: A thermal chamber is used to increase/decrease the ambient temperature. Unit is placed inside a box to prevent air flow.

Test Condition: Soak for 15 minutes and 5 minutes for each line/step. Measured across PCB output terminals.

8.2.1 5 V and 12 V Output at Full Load Condition (uVCC = 3.3 V / 0 A)

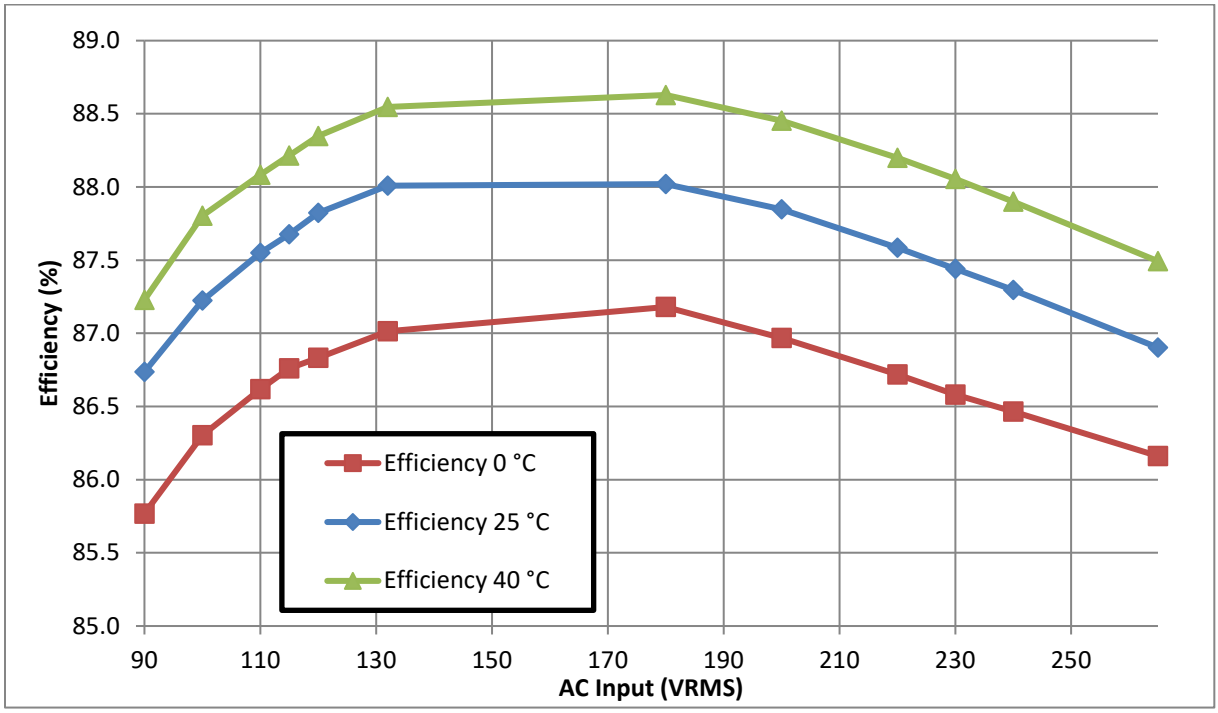


Figure 8 – Full load Efficiency vs. Line Voltage (uVCC = 3.3 V / 0 A).

8.2.2 5 V and 12 V Output at Full Load Condition (uVCC = 3.3 V / 20 mA)

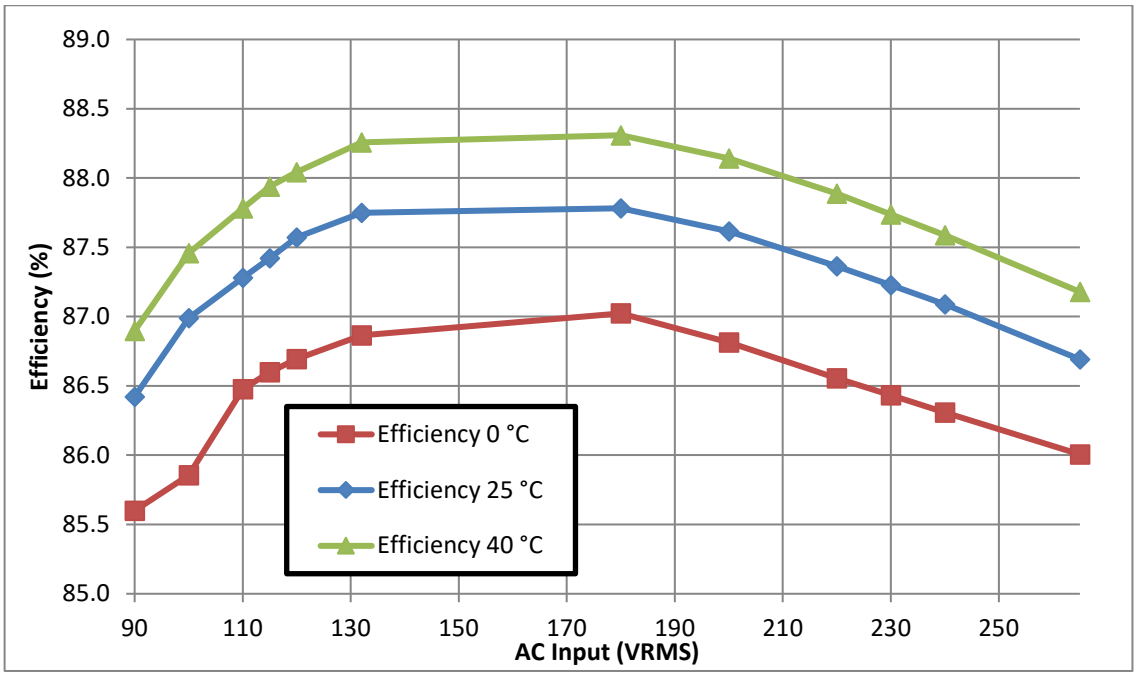


Figure 9 – Full load Efficiency vs. Line Voltage (uVCC = 3.3 V / 20 mA).

8.3 *Efficiency vs. Load*

Note: A thermal chamber is used to increase/decrease the ambient temperature. Unit is placed inside a box to prevent air flow.

Test Condition: Soak for 15 minutes and 2 minutes for each line/step. Measured across PCB output terminals.

8.3.1 Efficiency vs. Load (uVCC = 3.3 V / 0 A)

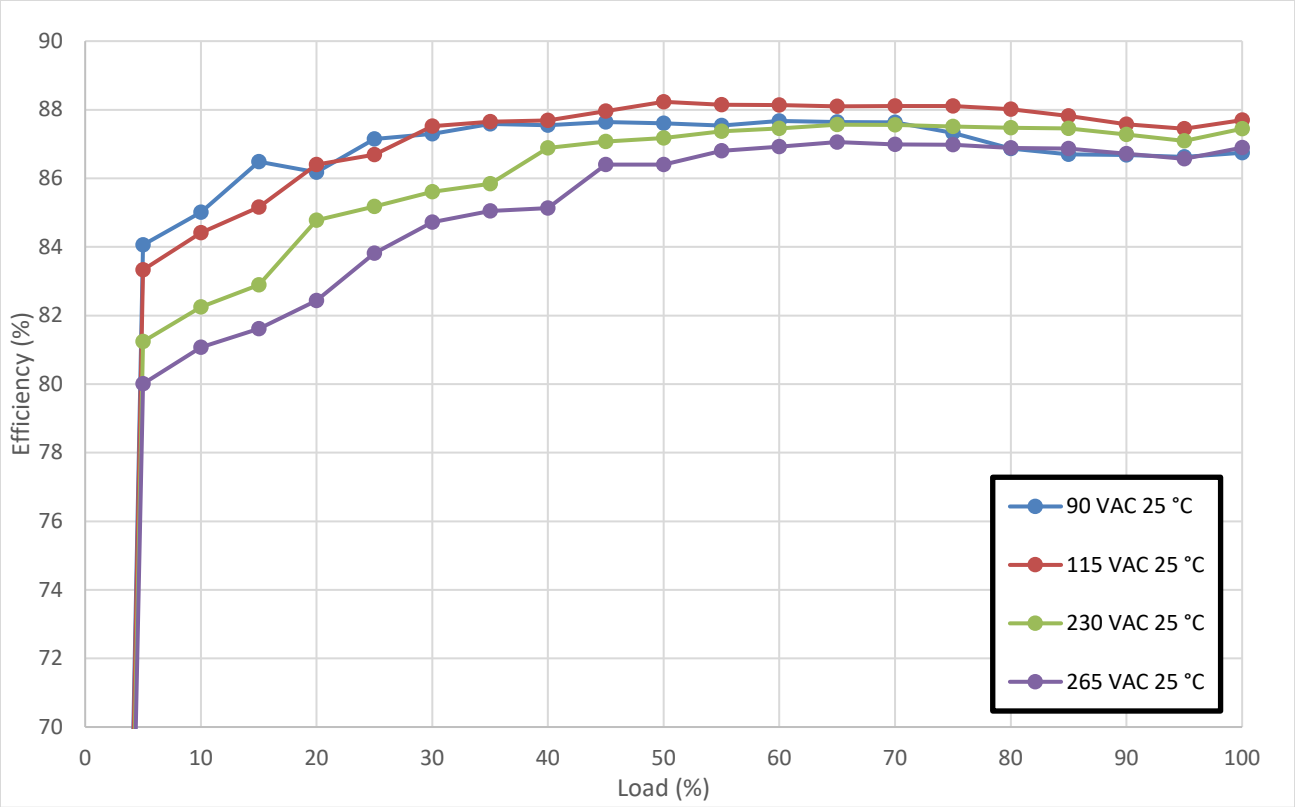


Figure 10 – Efficiency vs. Load, Room Ambient – 25 ºC Temperature.

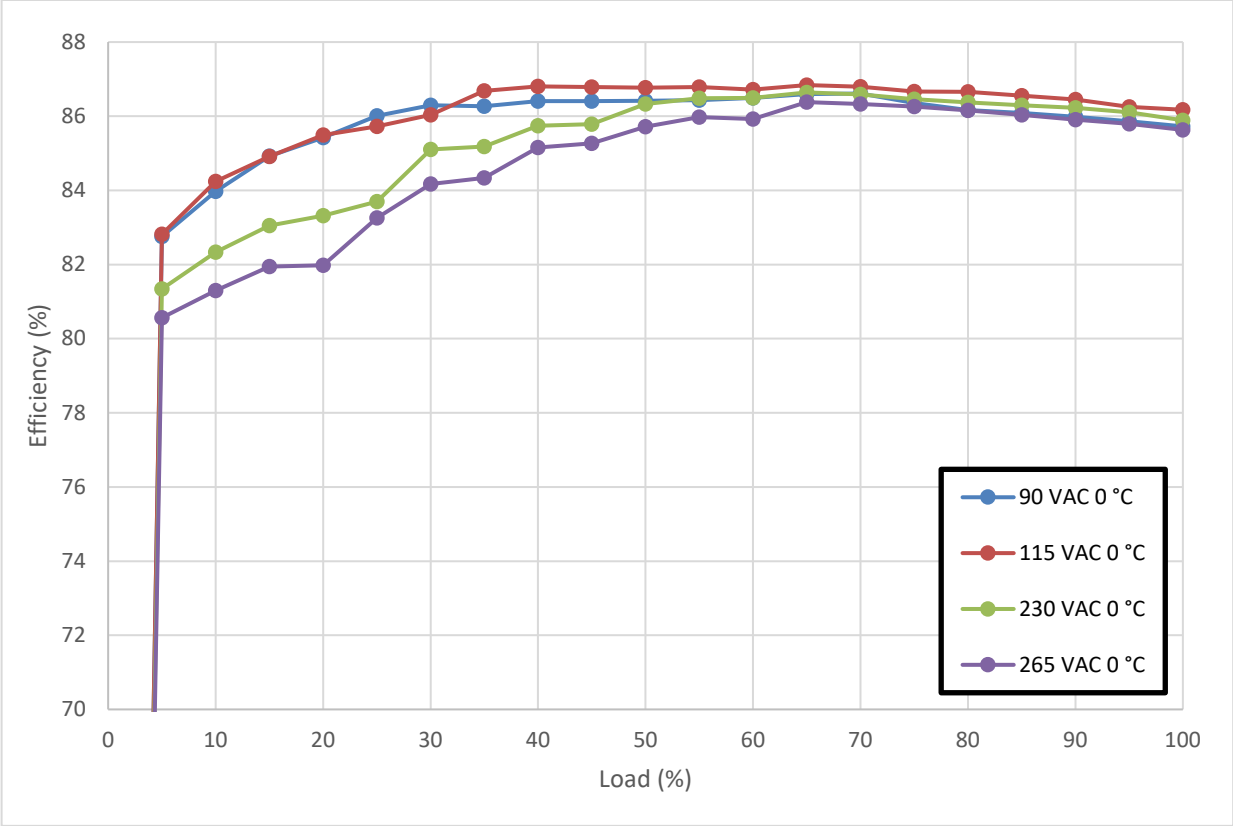


Figure 11 – Efficiency vs. Load, Cold Ambient – 0 ºC Temperature.

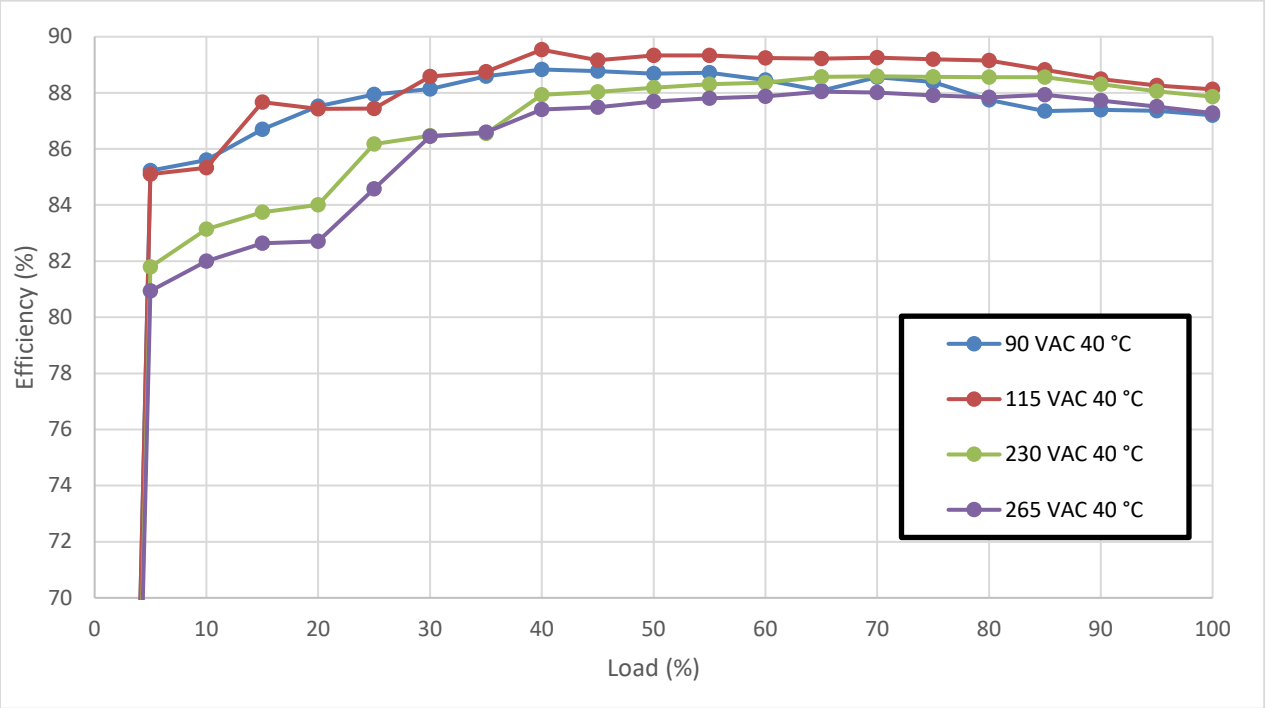


Figure 12 – Efficiency vs. Load, Hot Ambient – 40 ºC Temperature.

8.3.2 Efficiency vs. Load (uVCC = 3.3 V / 20 mA)

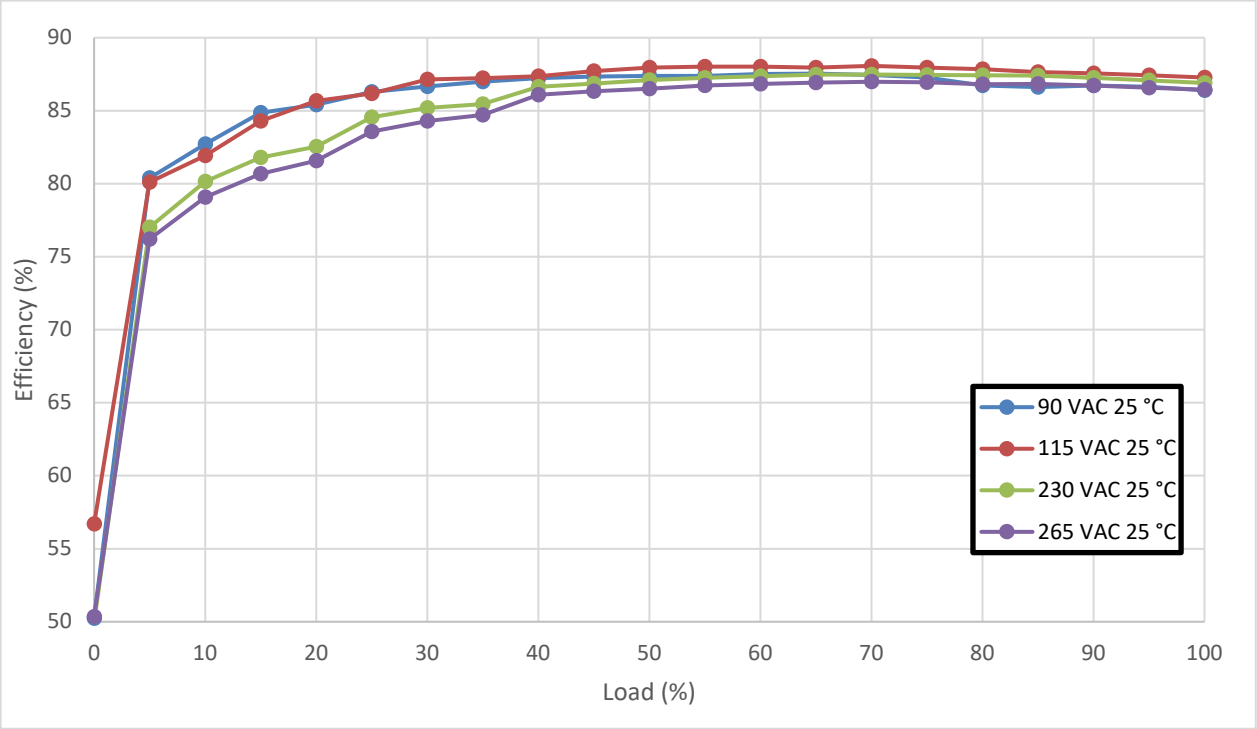


Figure 13 – Efficiency vs. Load, Room Ambient – 25 ºC Temperature.

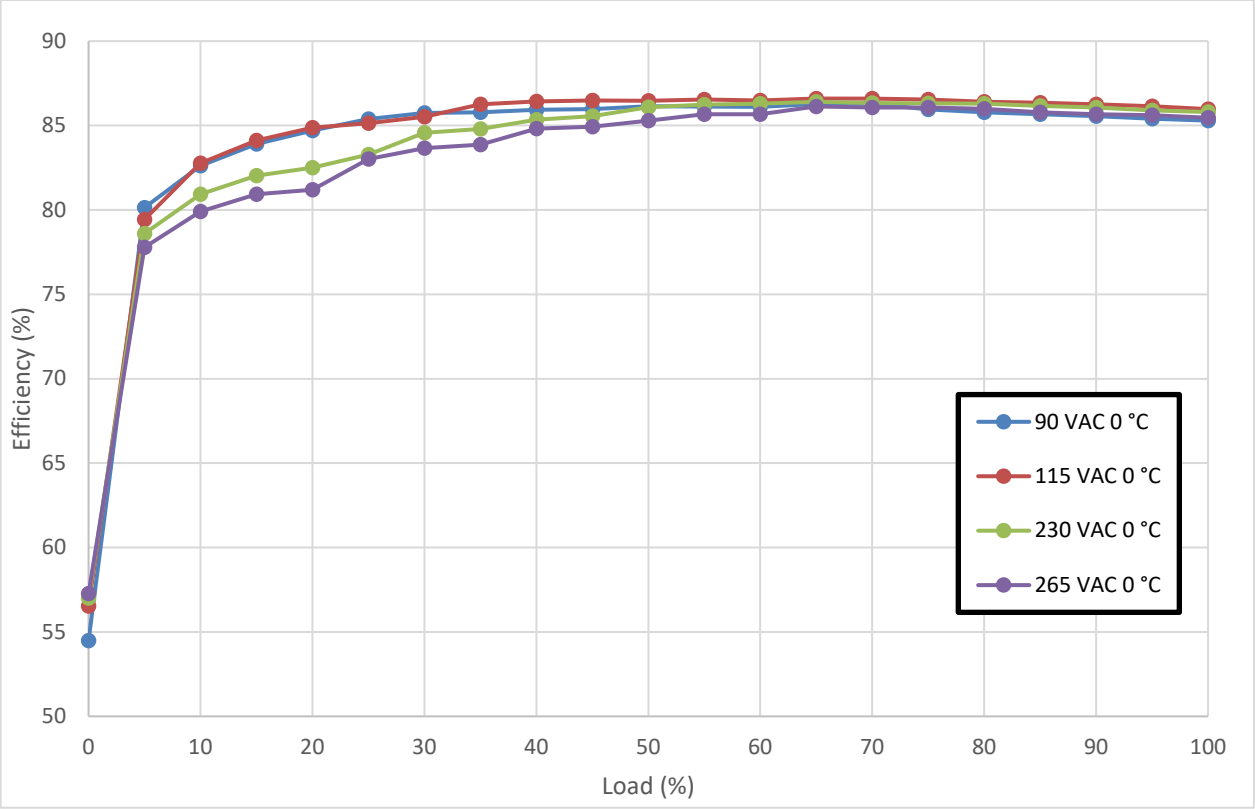


Figure 14 – Efficiency vs. Load, Cold Ambient – 0 ºC Temperature.

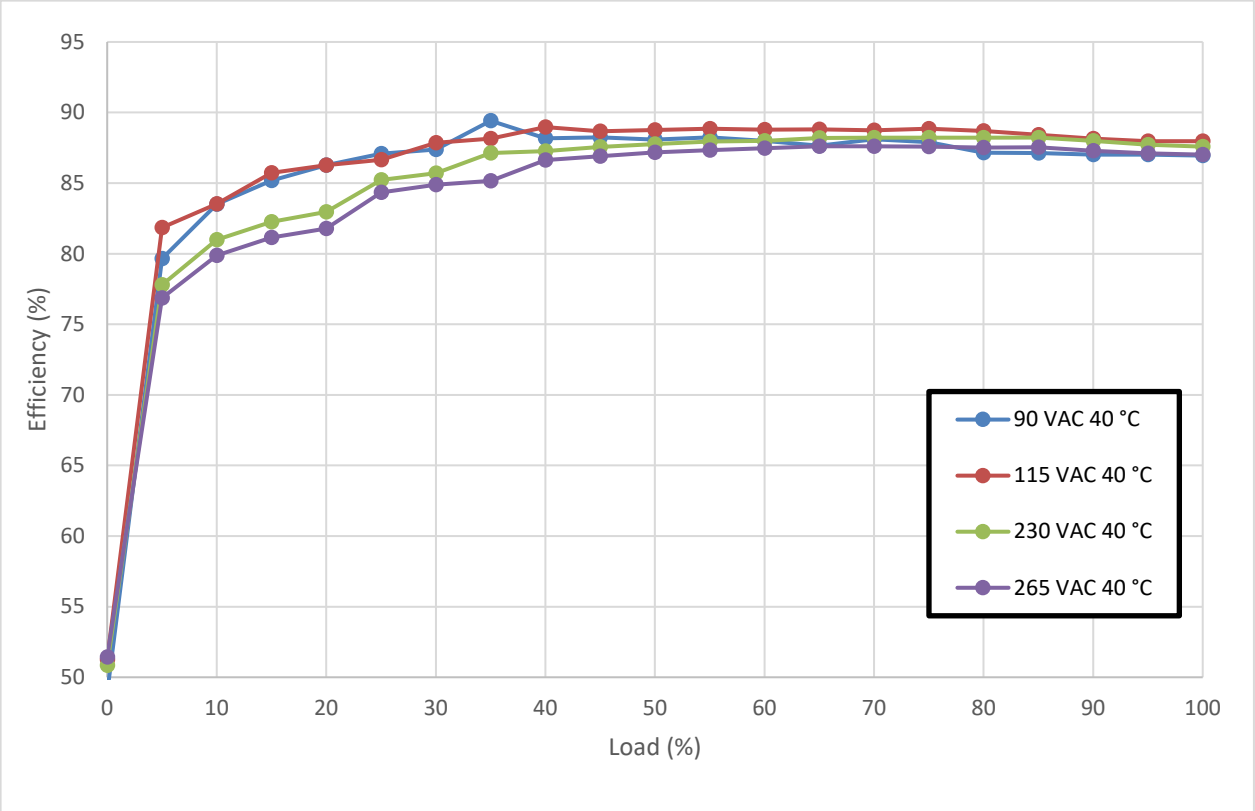


Figure 15 – Efficiency vs. Load, Hot Ambient – 40°C Temperature.

8.4 *No-Load Input Power*

Note: Soak for at least 15 minutes at full load then integrate for 15 minutes each line at no-load condition.

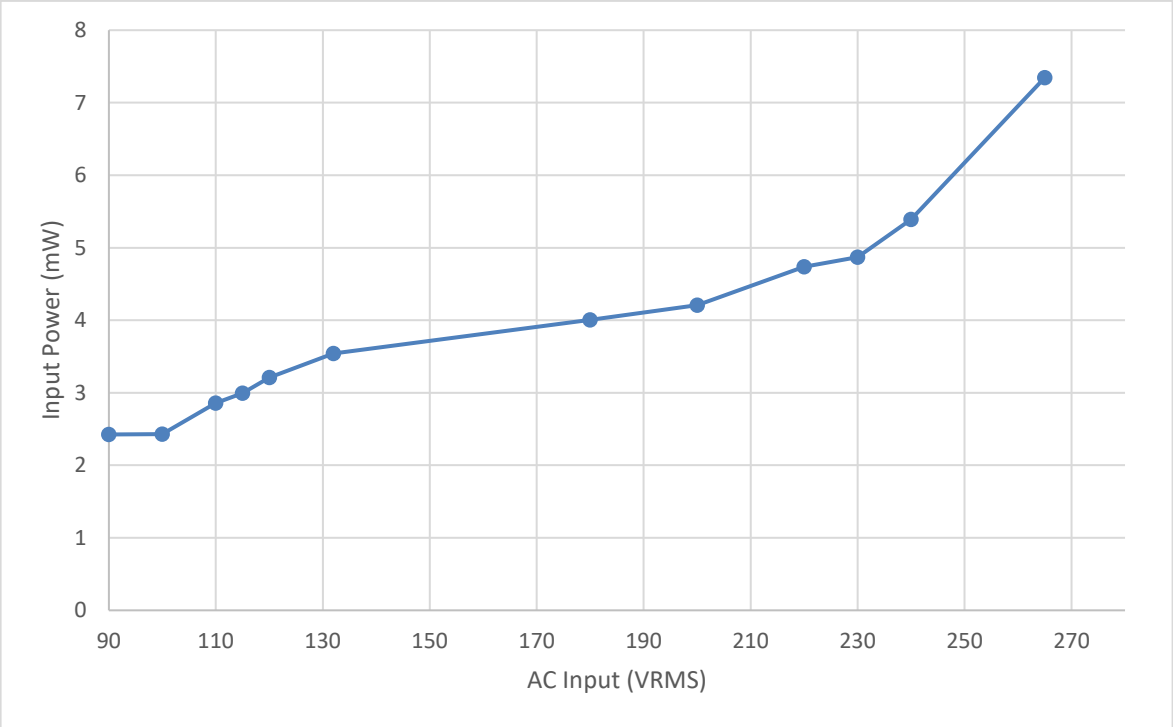


Figure 16 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

8.5 *Standby Input Power*

Test Condition: Soak at full load for 5 minutes and decrease the load to standby mode for 5 minutes each line step.

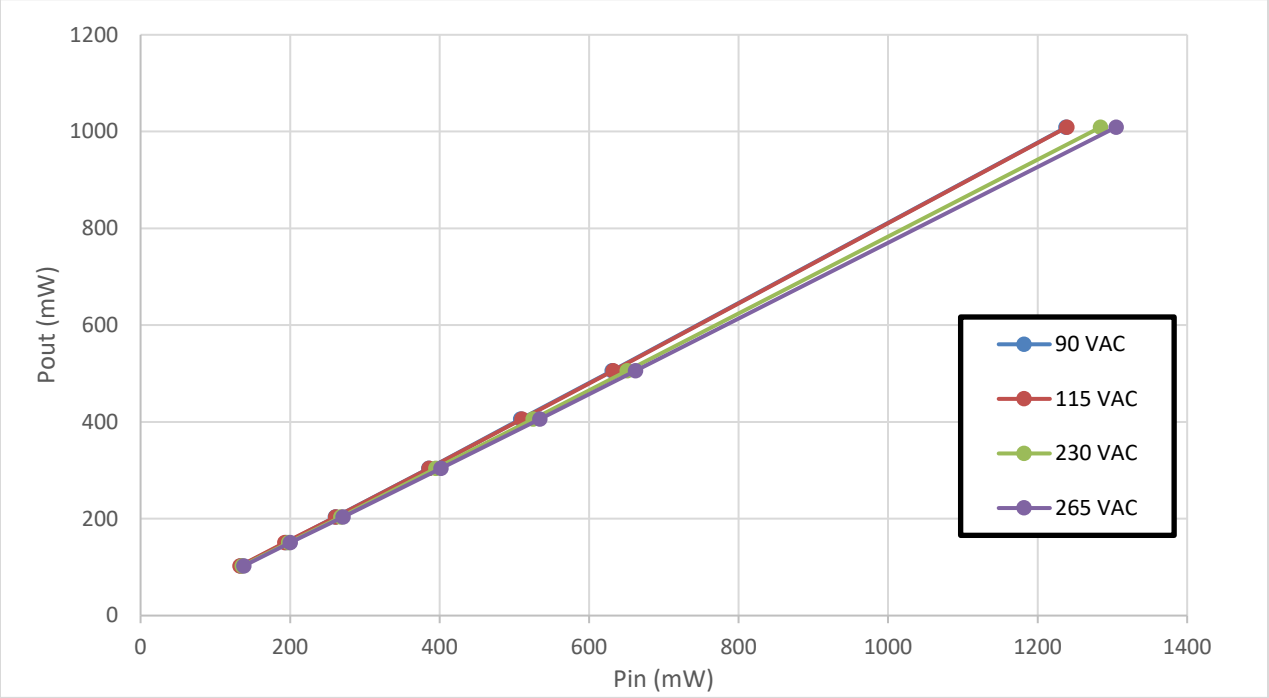


Figure 17 – Standby Input Power vs. Output Power.

8.5.1 Standby Efficiency

8.5.1.1 90 VAC

V_{IN} (V_{RMS})	I_{IN} (mA)	P_{IN} (mW)	$5V_{OUT}$ (V_{DC})	$5I_{OUT}$ (mA_{DC})	5Pout (mW)	Efficiency (%)
90	27.06	**1238**	4.91	205.30	**1008.64**	**81.47**
90	14.13	**630.9**	4.92	102.80	**505.57**	**80.13**
90	11.50	**508.4**	4.92	82.50	**405.90**	**79.84**
90	8.85	**385.4**	4.92	61.80	**304.30**	**78.96**
90	6.13	**260.7**	4.93	41.30	**203.53**	**78.07**
90	4.673	**194.5**	4.93	30.60	**150.83**	**77.55**
90	3.318	**133.9**	4.93	20.80	**102.59**	**76.61**

8.5.1.2 115 VAC

V_{IN} (V_{RMS})	I_{IN} (mA)	P_{IN} (mW)	$5V_{OUT}$ (V_{DC})	$5I_{OUT}$ (mA_{DC})	5Pout (mW)	Efficiency (%)
115	21.54	**1239**	4.91	205.30	**1008.84**	**81.42**
115	11.26	**632**	4.92	102.80	**505.57**	**80.00**
115	9.18	**510**	4.92	82.50	**405.90**	**79.59**
115	7.05	**386**	4.92	61.80	**304.18**	**78.80**
115	4.9	**261**	4.93	41.30	**203.44**	**77.95**
115	3.69	**193**	4.93	30.60	**150.83**	**78.15**
115	2.61	**133**	4.93	20.80	**102.59**	**77.13**

8.5.1.3 230 VAC

V_{IN} (V_{RMS})	I_{IN} (mA)	P_{IN} (mW)	$5V_{OUT}$ (V_{DC})	$5I_{OUT}$ (mA_{DC})	5Pout (mW)	Efficiency (%)
230	11.56	**1284**	4.91	205.30	**1008.84**	**78.57**
230	6.05	**651**	4.92	102.80	**505.67**	**77.68**
230	4.94	**525**	4.92	82.50	**405.98**	**77.33**
230	3.78	**395**	4.92	61.80	**304.30**	**77.04**
230	2.63	**268**	4.93	41.30	**203.49**	**75.93**
230	1.99	**198**	4.93	30.60	**150.83**	**76.18**
230	1.39	**136**	4.93	20.80	**102.59**	**75.43**

8.5.1.4 265 VAC

V_{IN} (V_{RMS})	I_{IN} (mA)	P_{IN} (mW)	$5V_{OUT}$ (V_{DC})	$5I_{OUT}$ (A_{DC})	5Pout (W)	Efficiency (%)
265	10.26	**1305**	4.92	205.30	**1009.05**	**77.32**
265	5.37	**662**	4.92	102.80	**505.67**	**76.39**
265	4.38	**534**	4.92	82.50	**405.98**	**76.03**
265	3.34	**402**	4.92	61.80	**304.30**	**75.70**
265	2.32	**271**	4.93	41.30	**203.49**	**75.09**
265	1.75	**200**	4.93	30.60	**150.86**	**75.43**
265	1.23	**138**	4.93	20.80	**102.61**	**74.35**

8.5.2 Available Standby Power

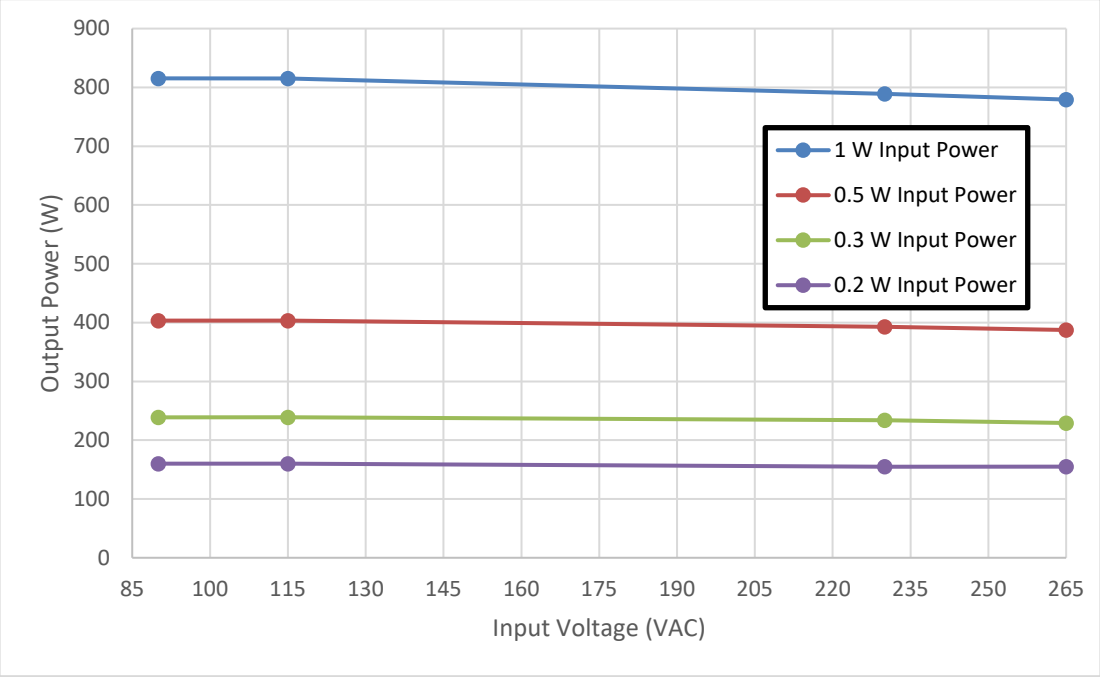


Figure 18 - Available Standby Output Power for 0.2 W, 0.3 W, 0.5 W and 1 W Input Power.

8.6 *Line and Load Regulation*

Note: A thermal chamber is used to increase/decrease the ambient temperature. Unit is placed inside a box to prevent air flow.

Test Condition: Soak for 15 minutes and 5 minutes for each line/step. Measured across PCB output terminals.

8.6.1 Line Regulation at Full Load Condition (uVCC = 3.3 V / 0 A)

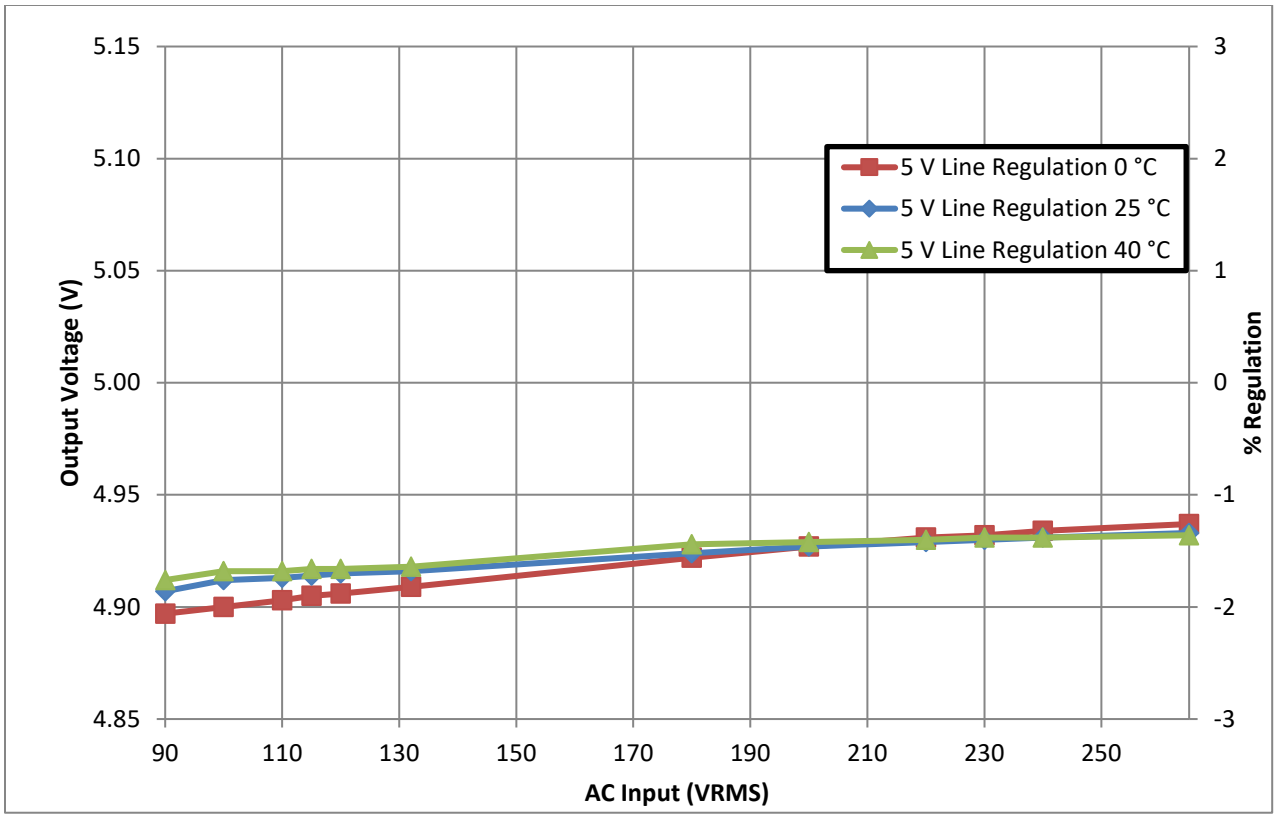


Figure 19 – 5 V Output Voltage vs. Input Line Voltage.

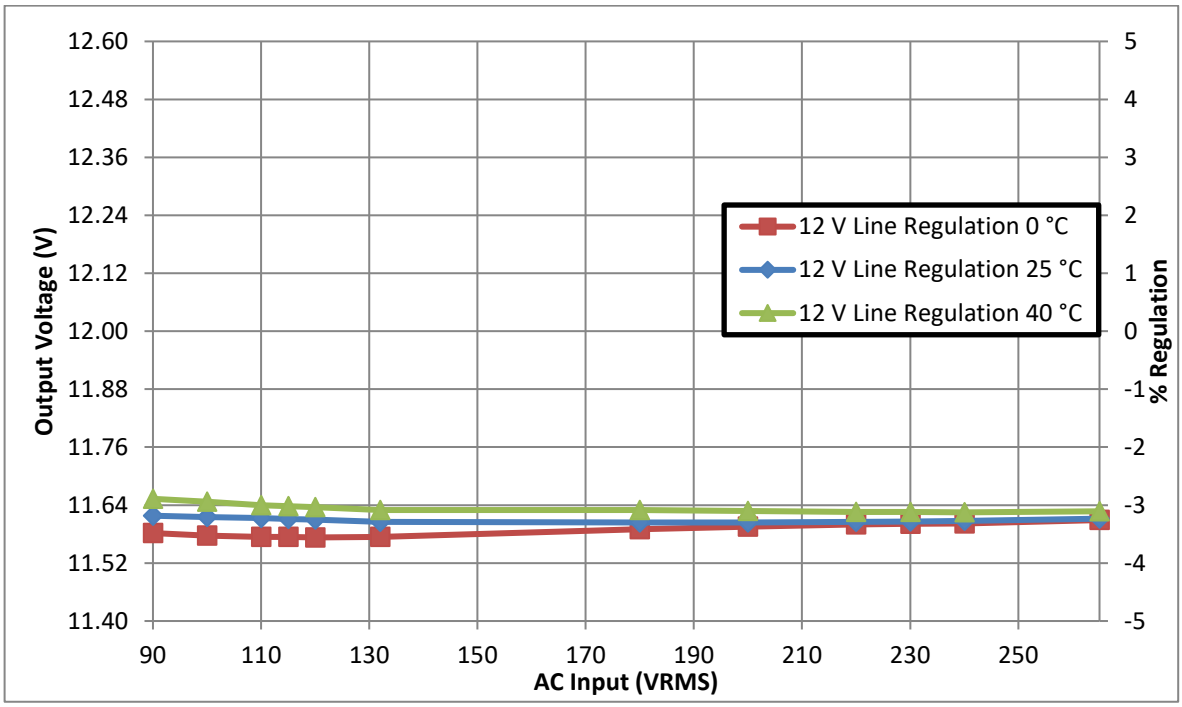


Figure 20 – 12 V Output Voltage vs. Input Line Voltage.

	5 V	12 V
Min.	4.94 V	11.65 V
Max.	4.90 V	11.58 V

8.6.2 Line Regulation at Full Load Condition (uVCC = 3.3 V / 20 mA)

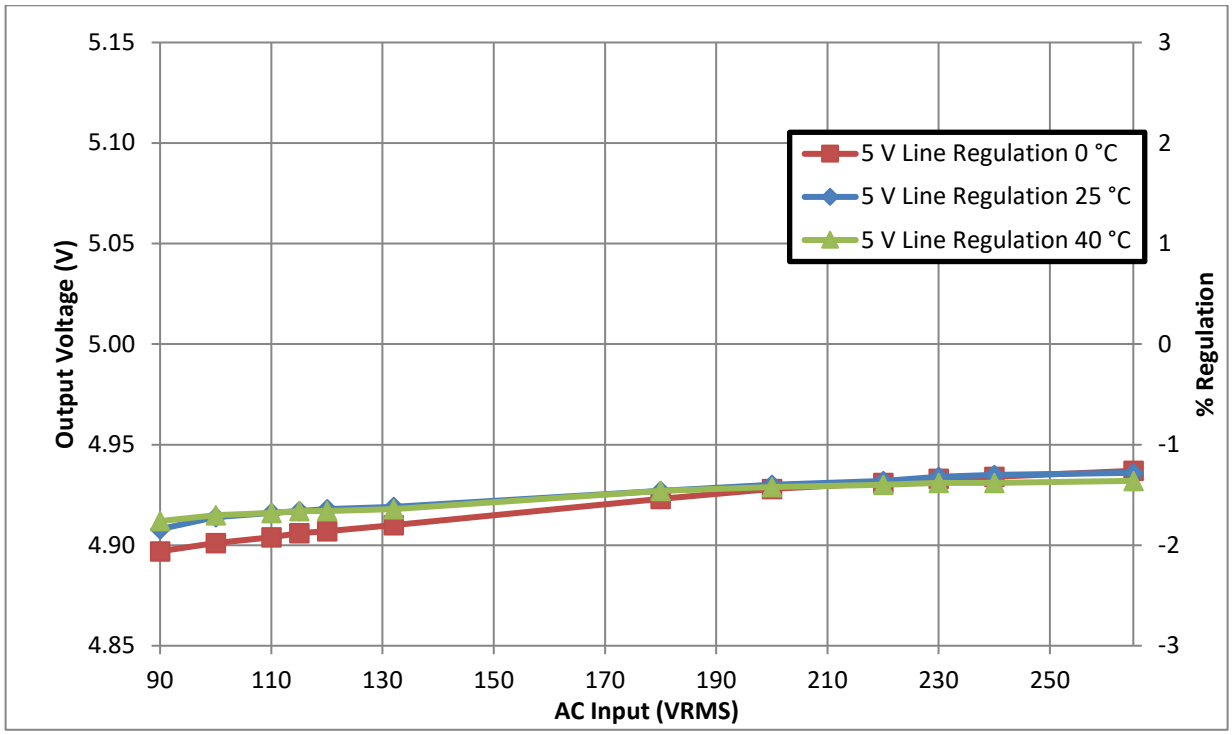


Figure 21 – 5 V Output Voltage vs. Input Line Voltage.

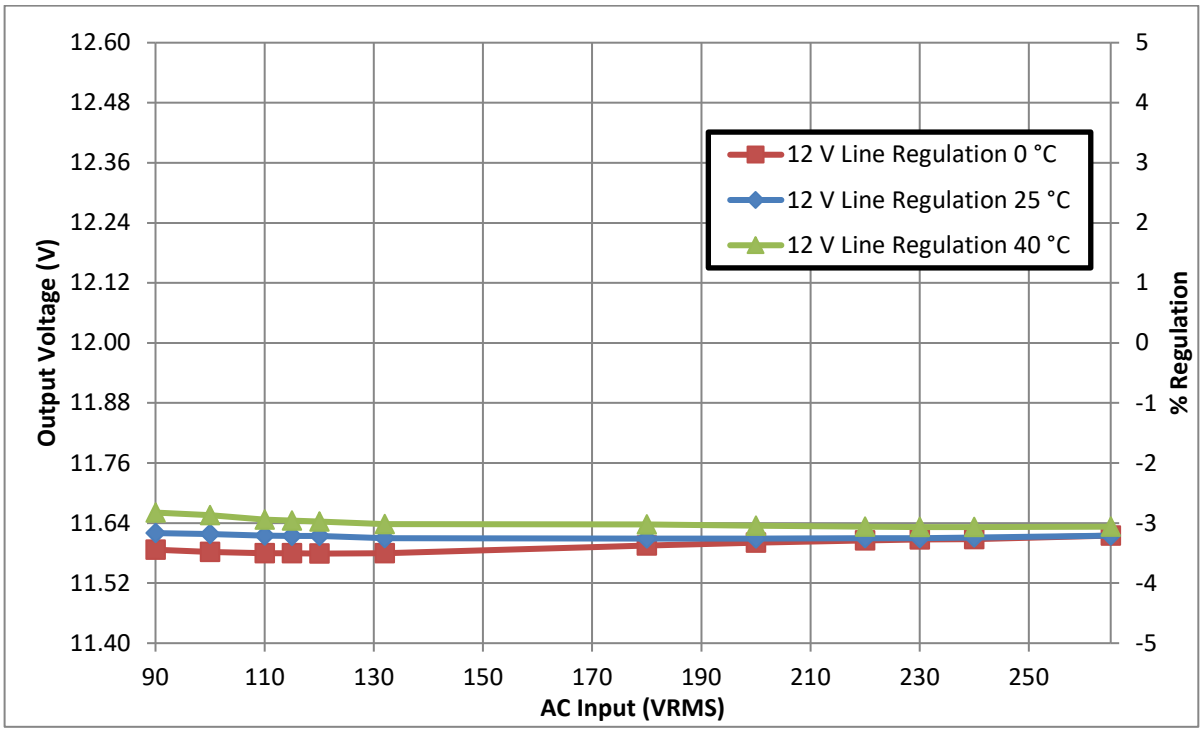


Figure 22 – 12 V Output Voltage vs. Input Line Voltage.

	5 V	12 V
Min.	4.94 V	11.66 V
Max.	4.90 V	11.59 V

8.6.3 5 V Load Regulation (uVCC = 3.3 V / 0 A)

Note: Both 5 V & 12 V outputs are loaded with the same percentage.

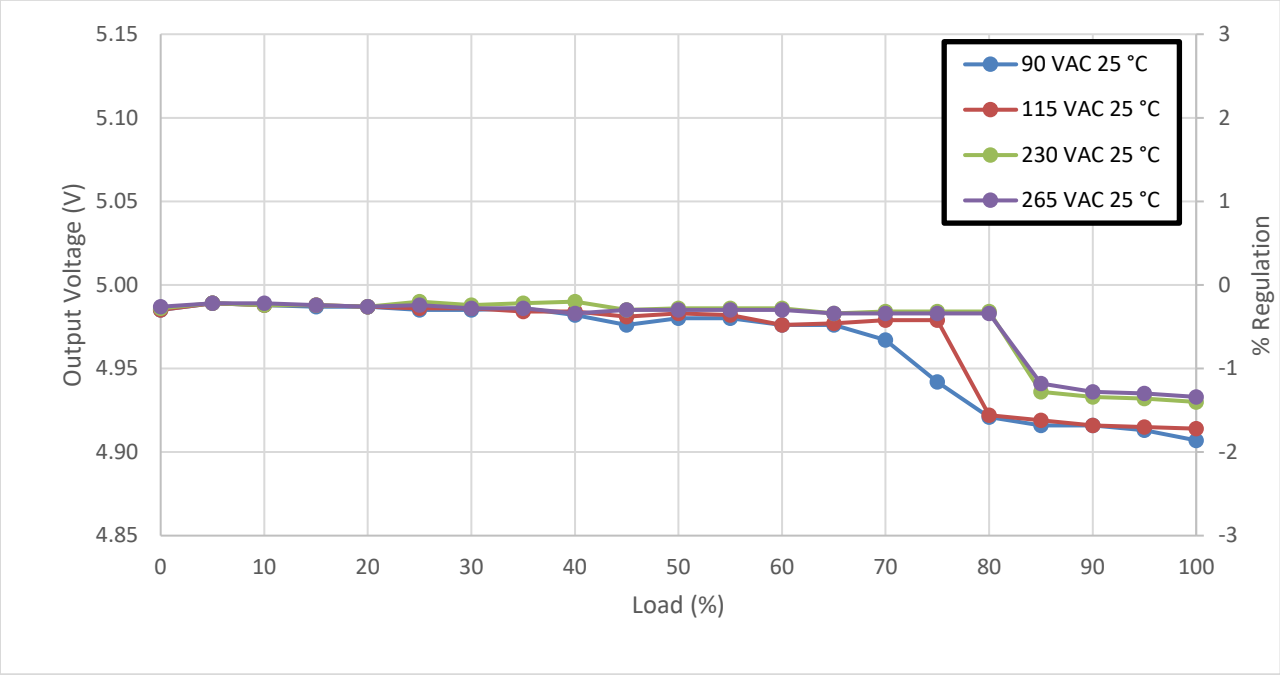


Figure 23 – 5 V Output Voltage vs. Load, Room Ambient – 25 ºC Temperature.

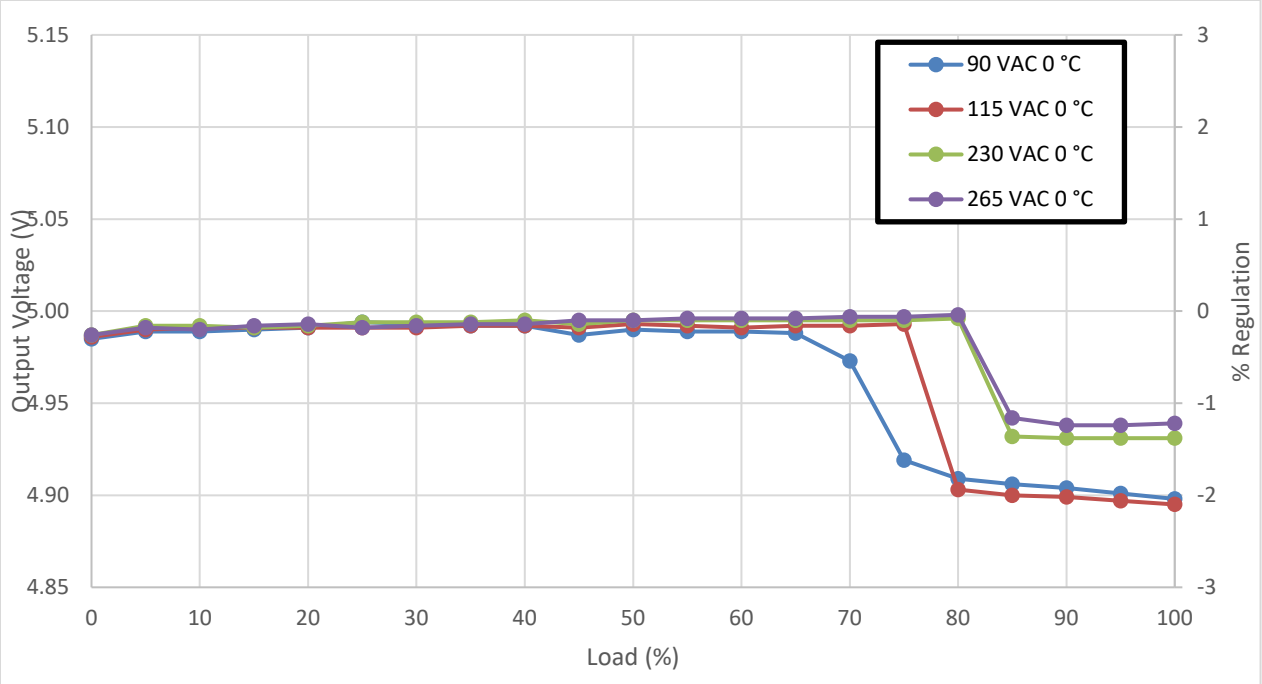


Figure 24 – 5 V Output Voltage vs. Load, Cold Ambient – 0 ºC Temperature.

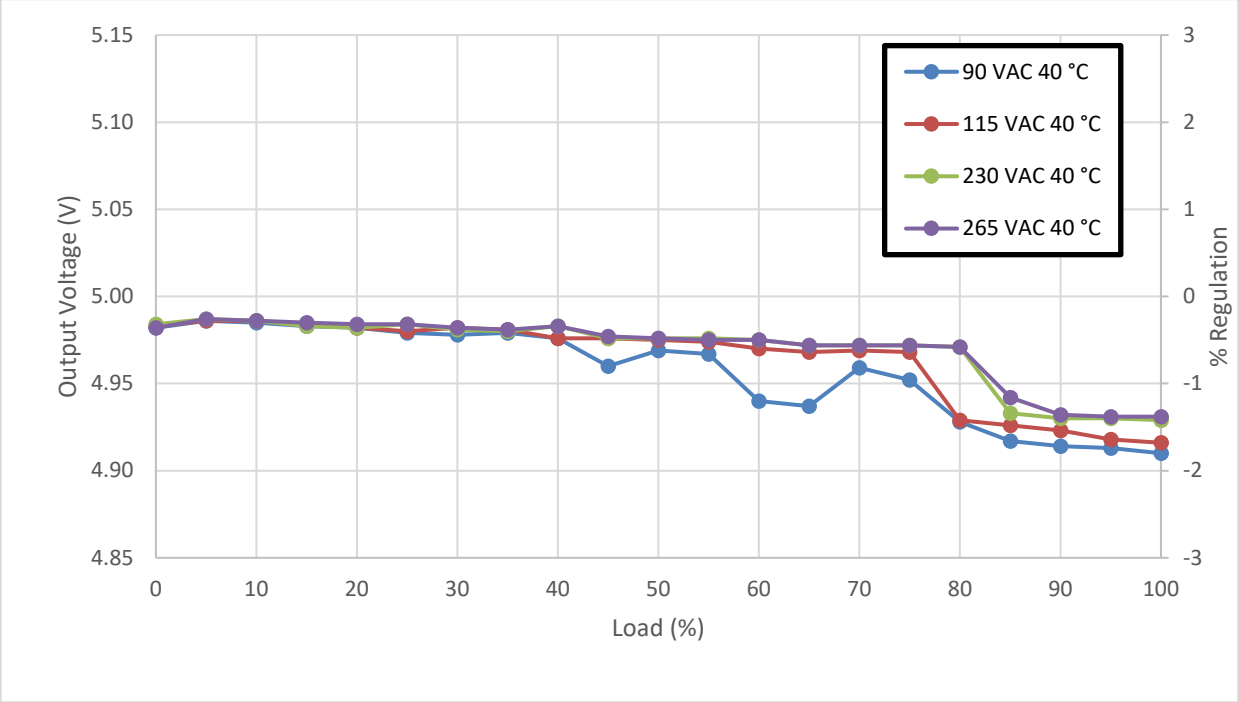


Figure 25 – 5 V Output Voltage vs. Load, Hot Ambient – 40 ºC Temperature.

8.6.4 5 V Load Regulation (uVCC = 3.3 V / 20 mA)

Note: Both 5 V & 12 V outputs are loaded with the same percentage.

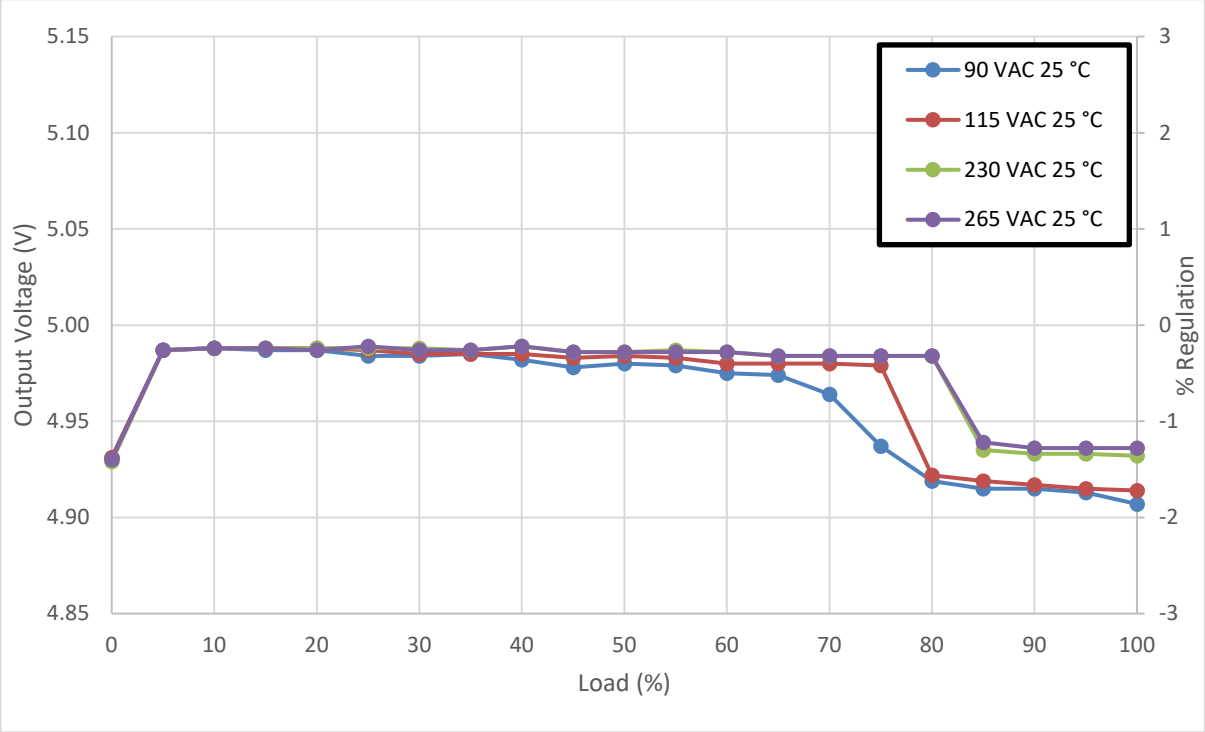


Figure 26 – 5 V Output Voltage vs. Load, Room Ambient – 25 ºC Temperature.

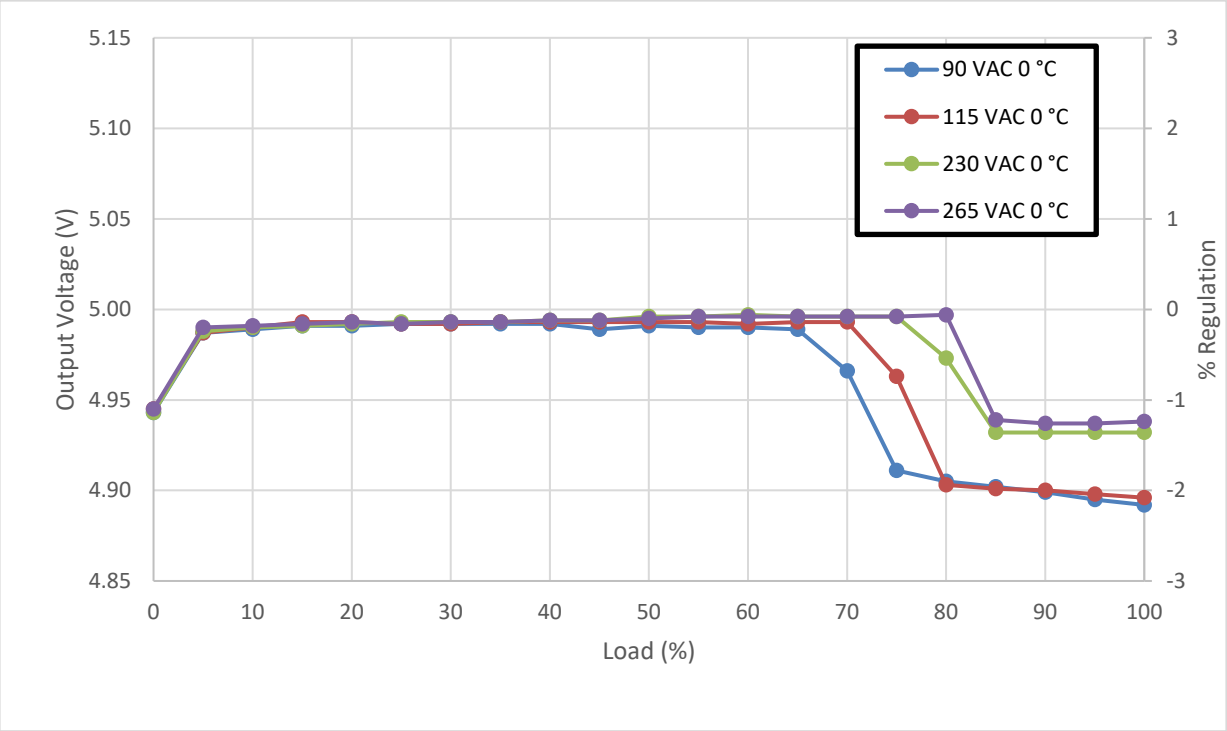


Figure 27 – 5 V Output Voltage vs. Load, Cold Ambient – 0 ºC Temperature.

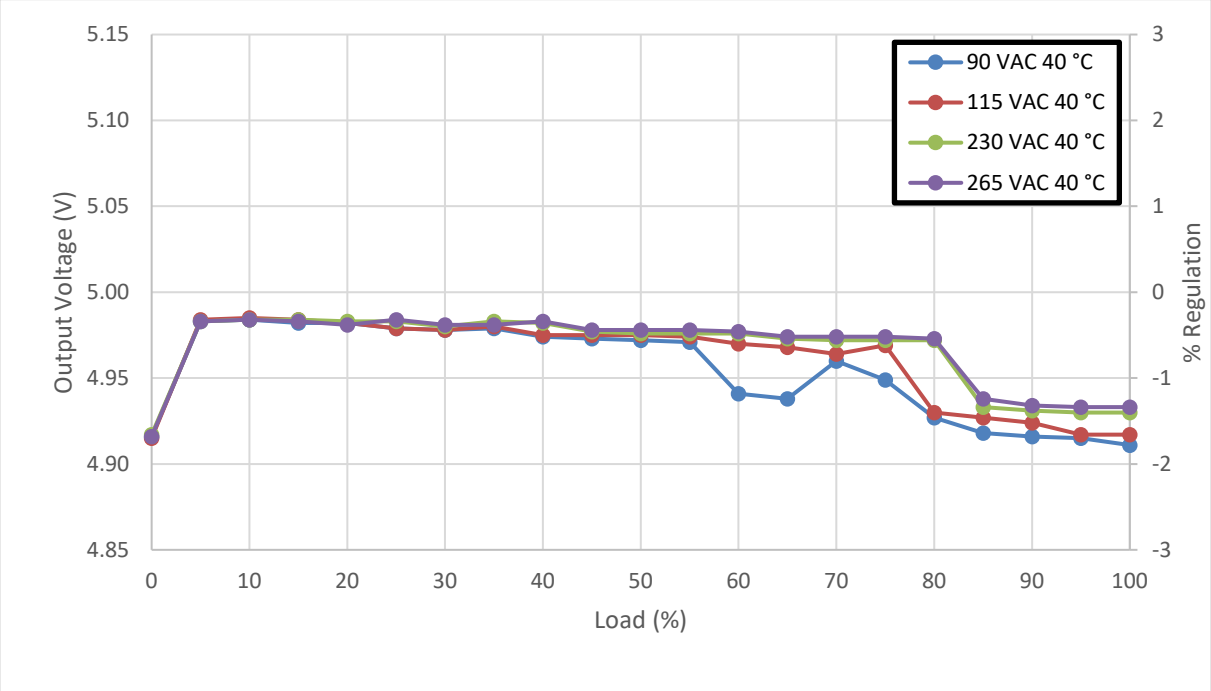


Figure 28 – 5 V Output Voltage vs. Load, Hot Ambient – 40 ºC Temperature.

8.6.5 12 V Load Regulation (uVCC = 3.3 V / 0 A)

Note: Both 5 V & 12 V outputs are loaded with the same percentage.

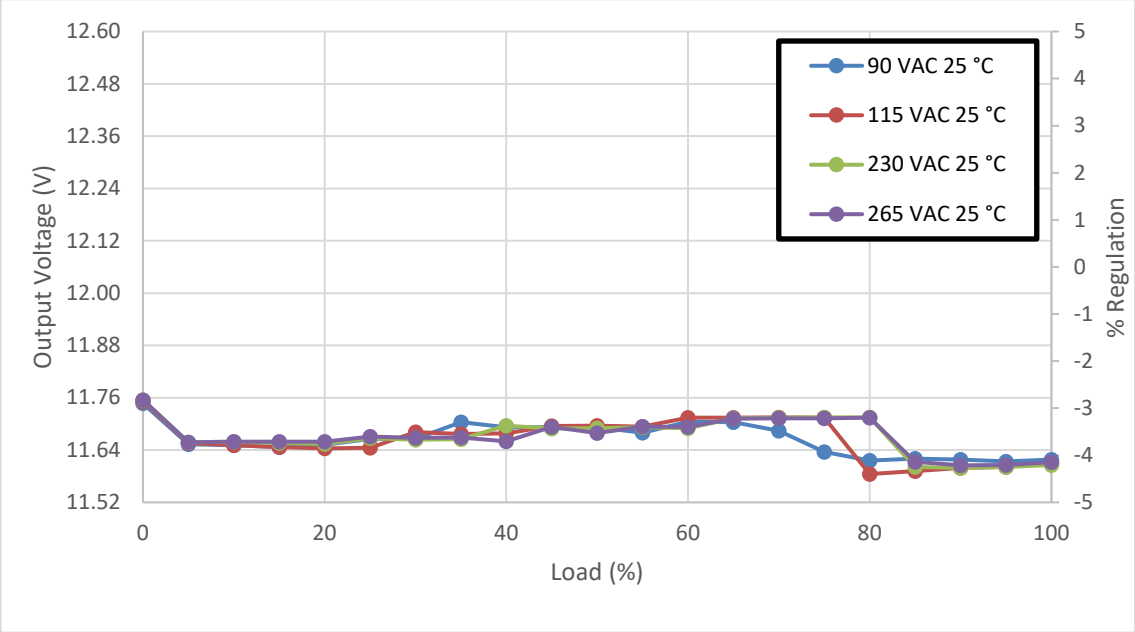


Figure 29 – 12 V Output Voltage vs. Load, Room Ambient – 25 ºC Temperature.

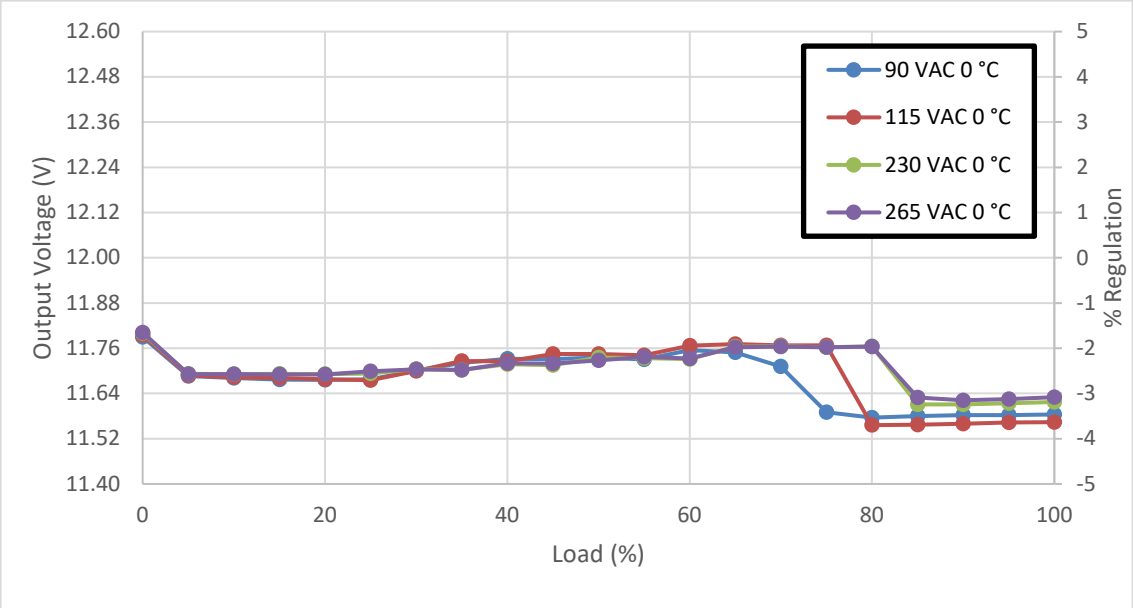


Figure 30 – 12 V Output Voltage vs. Load, Cold Ambient – 0 ºC Temperature.

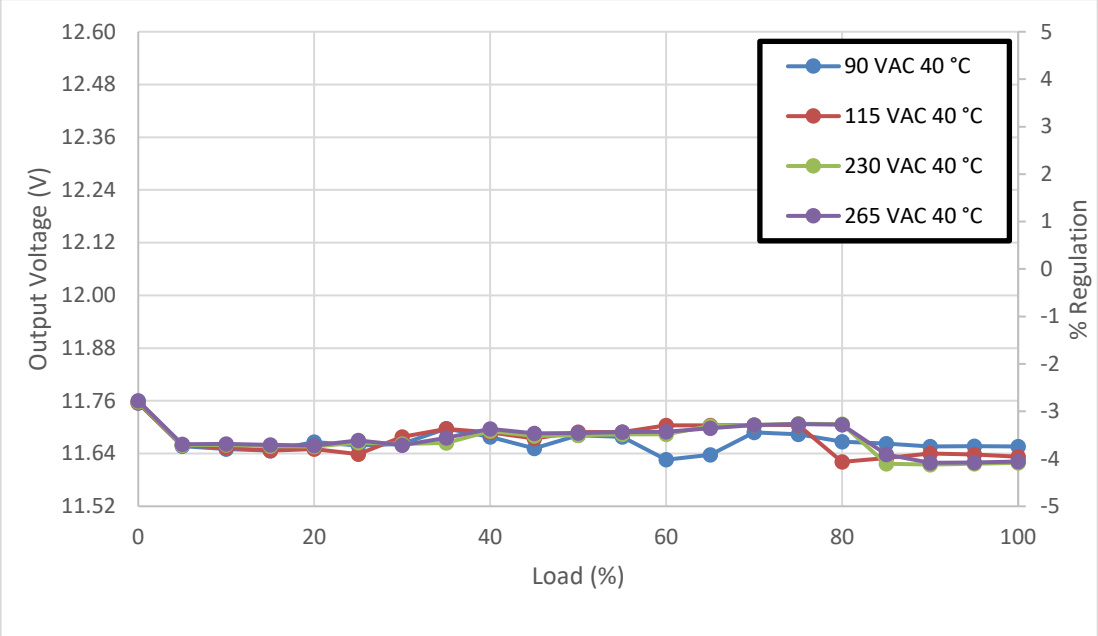


Figure 31 – 12 V Output Voltage vs. Load, Hot Ambient – 40 ºC Temperature.

8.6.6 12 V Load Regulation (uVCC = 3.3 V / 20 mA)

Note: Both 5 V & 12 V outputs are loaded with the same percentage.

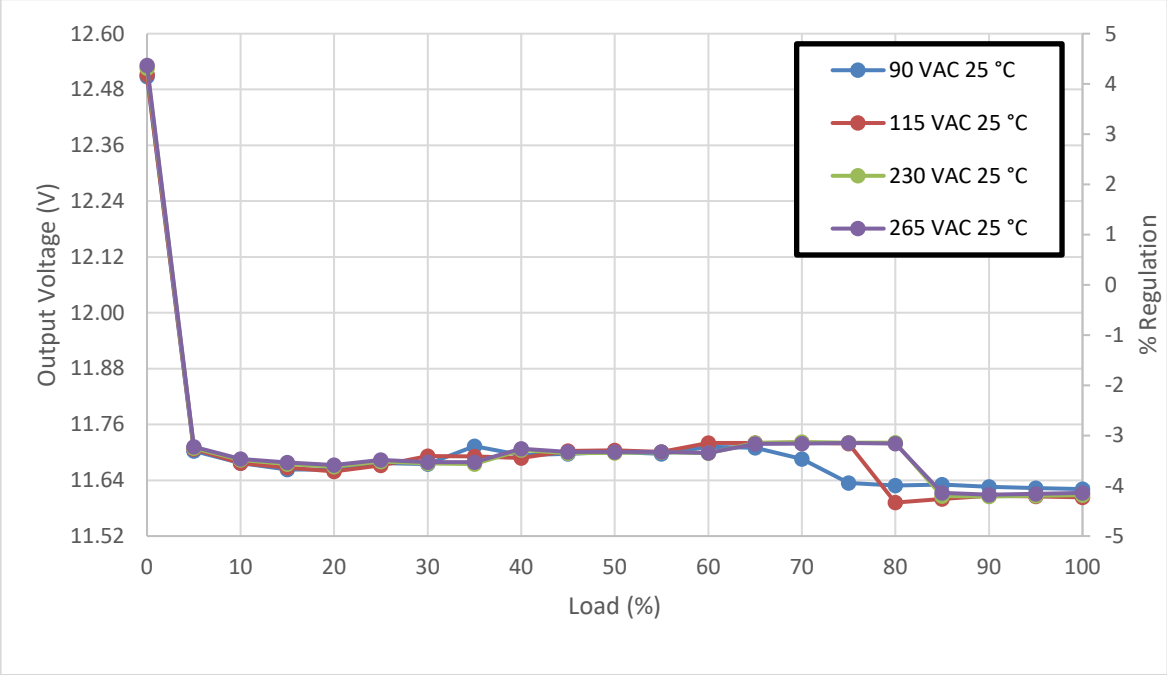


Figure 32 – 12 V Output Voltage vs. Load, Room Ambient – 25 ºC Temperature.

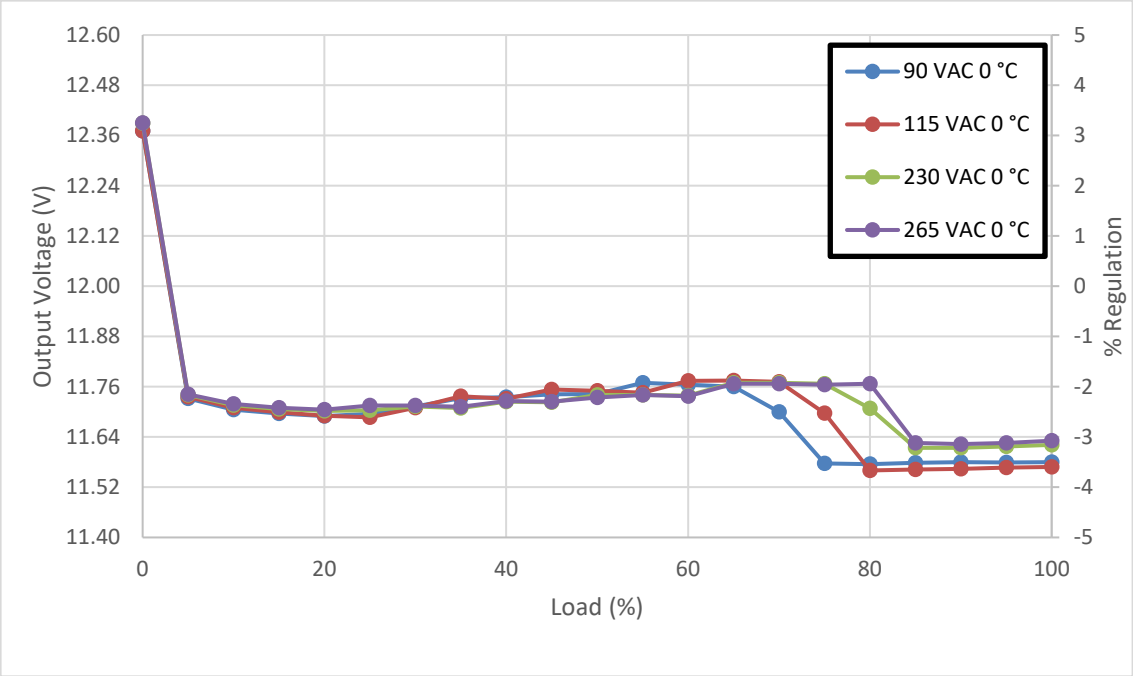


Figure 33 – 12 V Output Voltage vs. Load, Cold Ambient – 0 ºC Temperature.

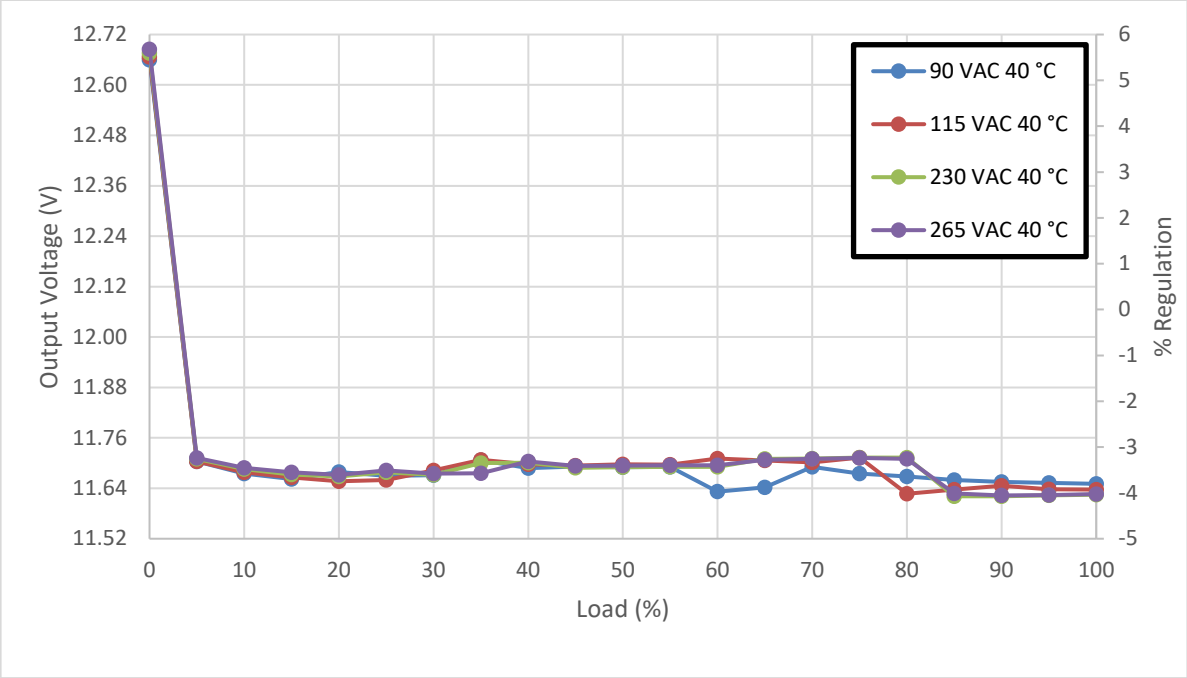


Figure 34 – 12 V Output Voltage vs. Load, Hot Ambient – 40 ºC Temperature.

8.7 *Cross Load Regulation*

8.7.1 12 V Load Change with Full Load on 5 V (uVCC = 3.3 V / 0 A)

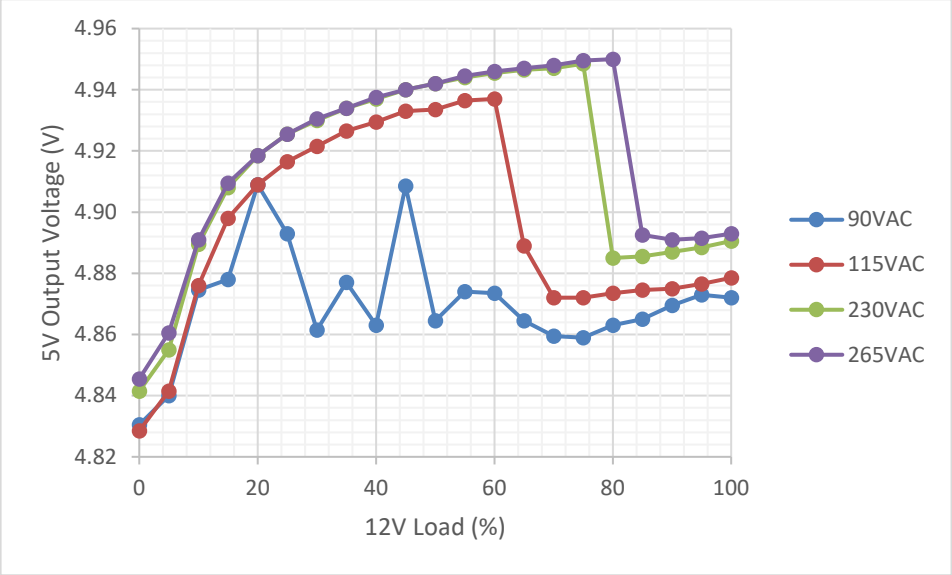


Figure 35 – 5 V Output Voltage While 12 V Output Load Change, 5 V at Full Load, Room Temperature.

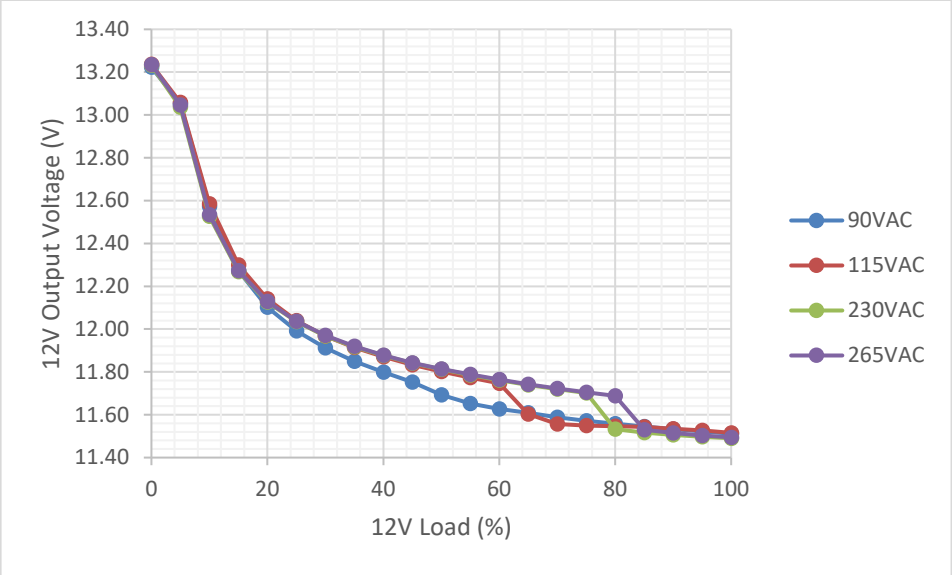


Figure 36 – 12 V Output Voltage While 12 V Output Load Change, 5 V at Full Load, Room Temperature.

	5 V	**12 V**
Max.	4.95	13.24
Min.	4.83	11.49

8.7.2 12 V Load Change with No-Load on 5 V (uVCC = 3.3 V / 0 A)

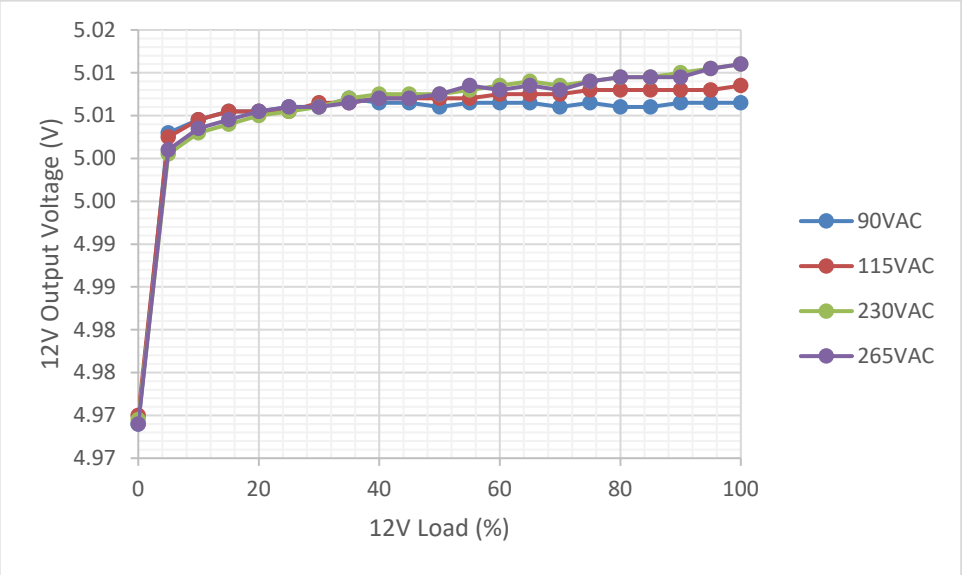


Figure 37 – 5 V Output Voltage While 12 V Output Load Change, 5 V at No-Load, Room Temperature.

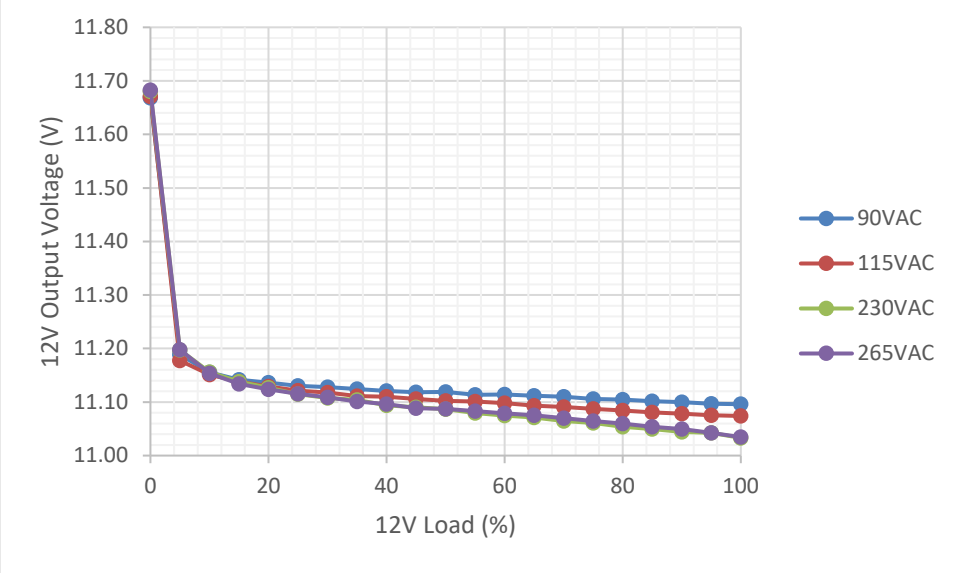


Figure 38 – 12 V Output Voltage While 12 V Output Load Change, 5 V at No-Load, Room Temperature.

	5 V	12 V
Max.	5.01	11.68
Min.	4.97	11.03

8.7.3 5 V Load Change with Full Load on 12 V (uVCC = 3.3 V / 0 A)

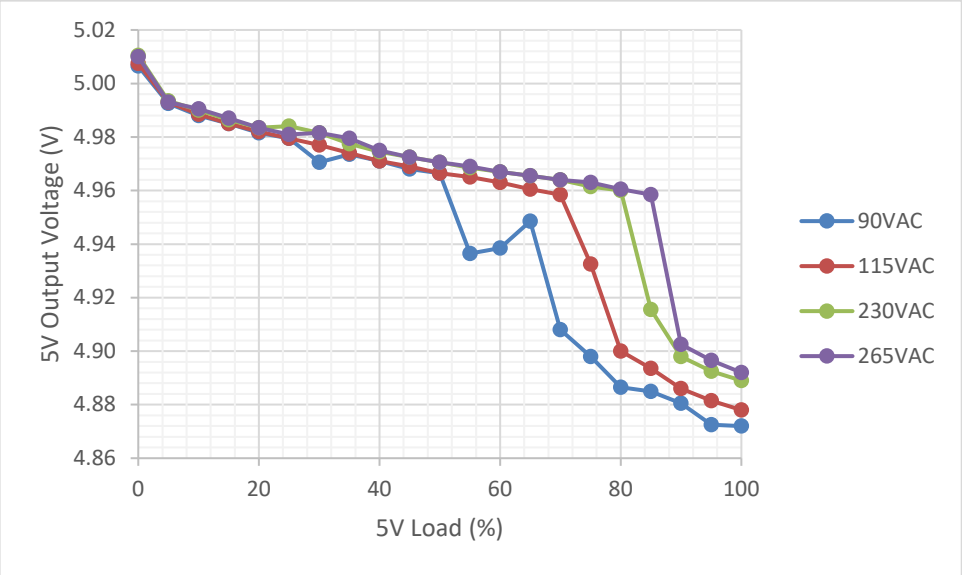


Figure 39 – 5 V Output Voltage while 5 V Output Load Change, 12 V at Full Load, Room Temperature.

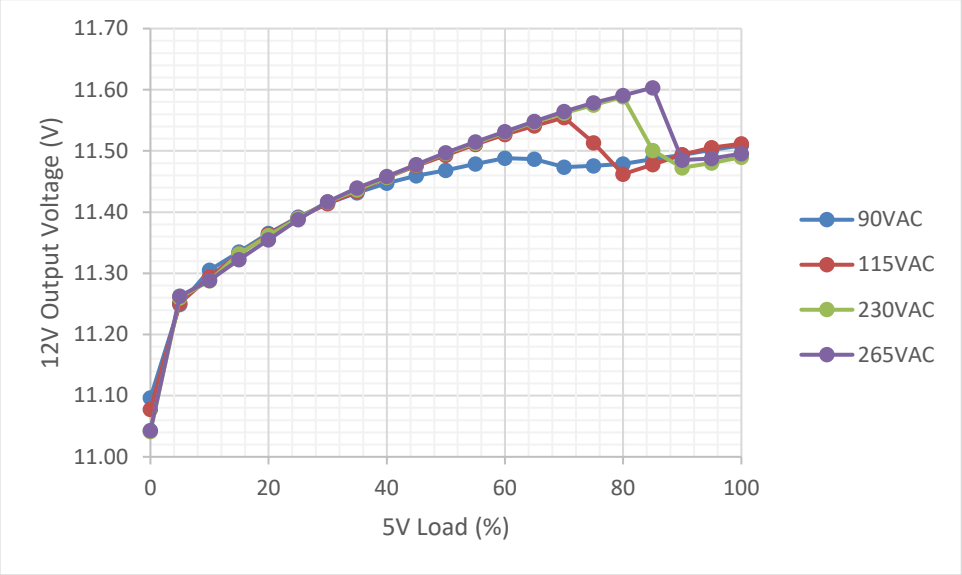


Figure 40 – 12 V Output Voltage while 5 V Output Load Change, 5 V at Full Load, Room Temperature.

	5 V	12 V
Max.	5.01	11.60
Min.	4.87	11.04

8.7.4 5 V Load Change with No-Load on 12 V (uVCC = 3.3 V / 0 A)

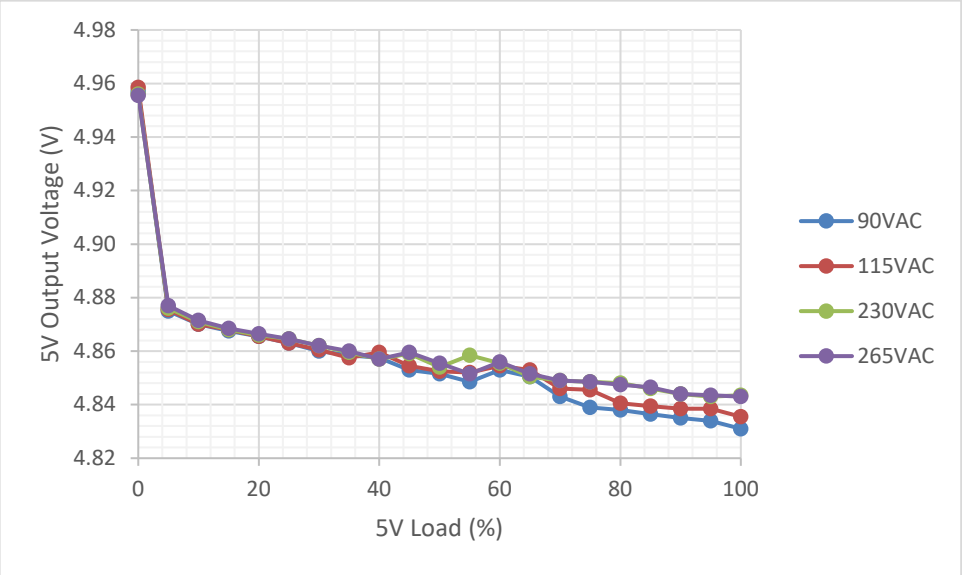


Figure 41 – 5 V Output Voltage while 5 V Output Load Change, 5 V at No-Load, Room Temperature.

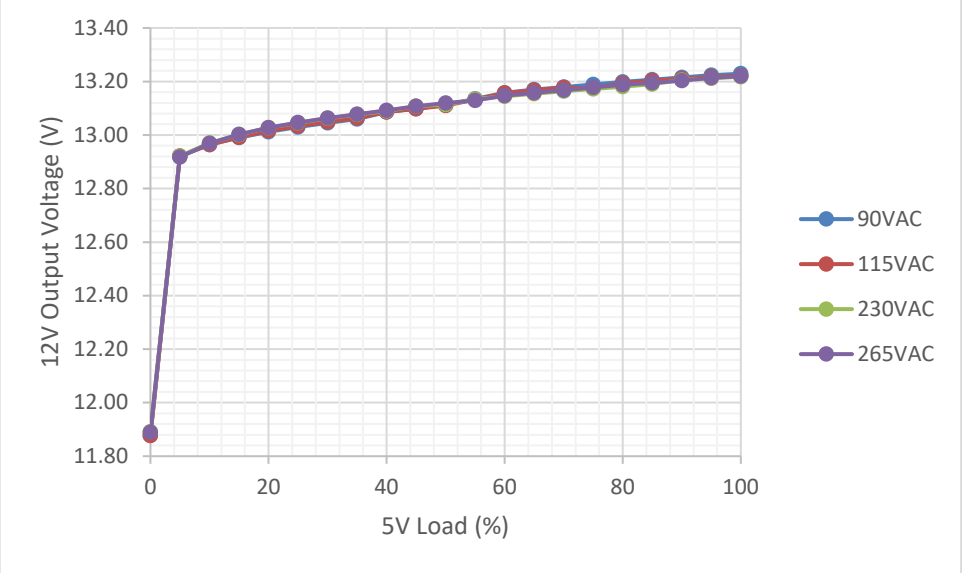


Figure 42 – 12 V Output Voltage while 5 V Output Load Change, 5 V at No-Load, Room Temperature.

	5 V	**12 V**
Max.	4.96	13.23
Min.	4.83	11.88

8.7.5 12 V Load Change with Full Load on 5 V (uVCC = 3.3 V / 20 mA)

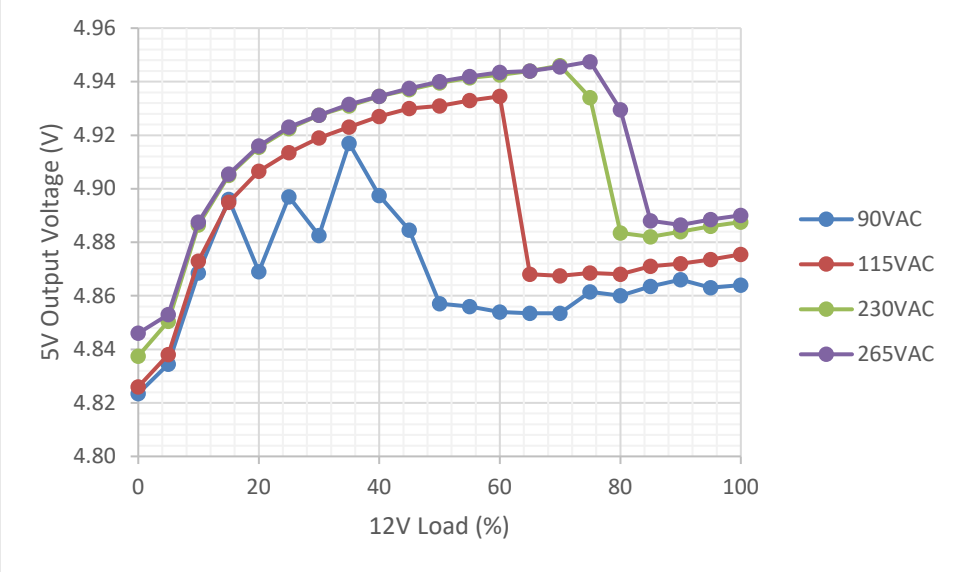


Figure 43 – 5 V Output Voltage While 12 V Output Load Change, 5 V at Full Load, Room Temperature.

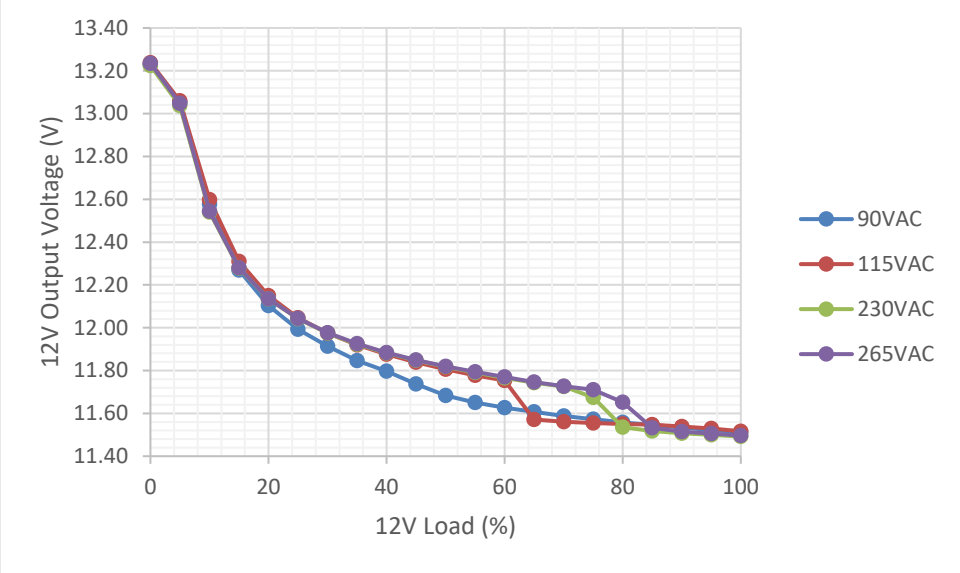


Figure 44 – 12 V Output Voltage While 12 V Output Load Change, 5 V at Full Load, Room Temperature.

	5 V	12 V
Max.	4.95	13.24
Min.	4.82	11.49

8.7.6 12 V Load Change with No-Load on 5 V (uVCC = 3.3 V / 20 mA)

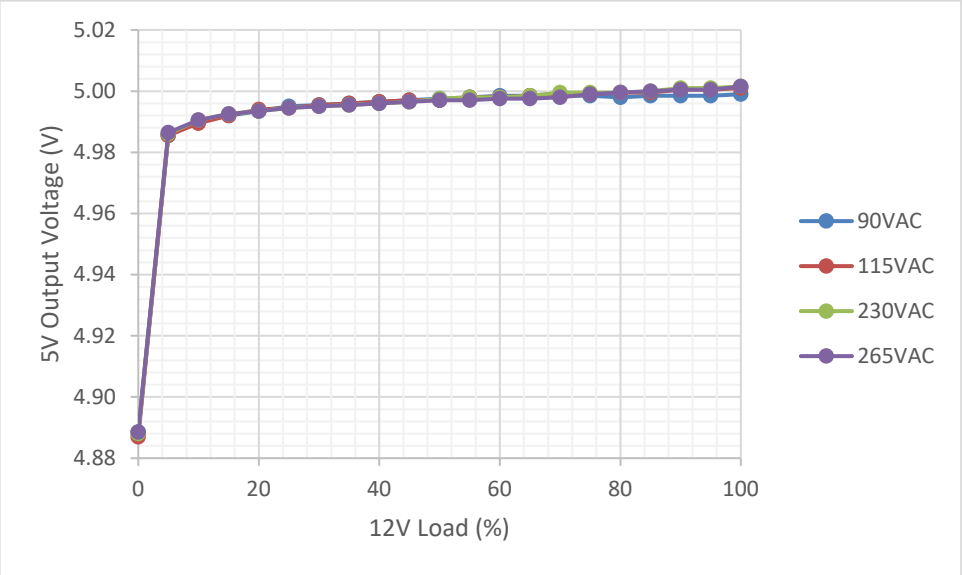


Figure 45 – 5 V Output Voltage While 12 V Output Load Change, 5 V at No-Load, Room Temperature.

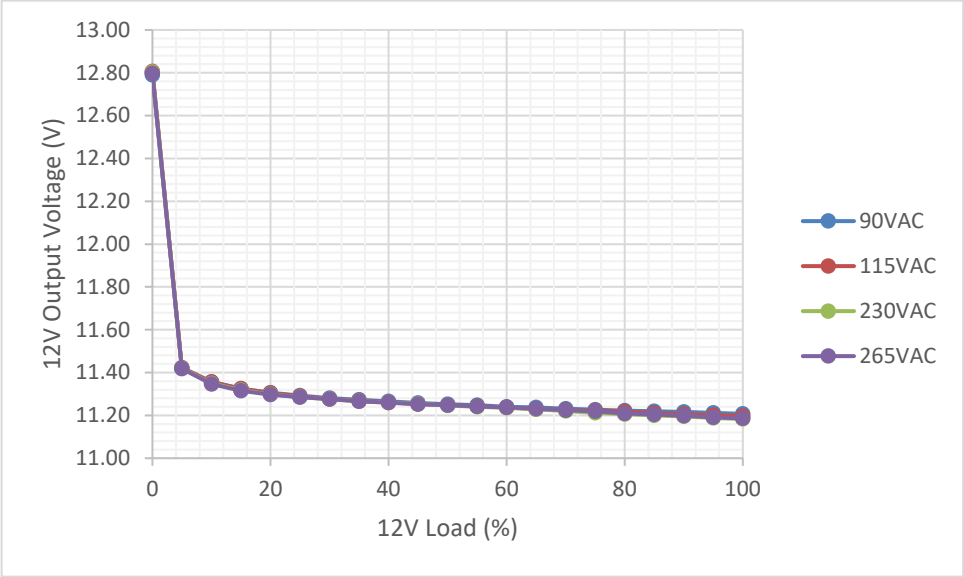


Figure 46 – 12 V Output Voltage While 12 V Output Load Change, 5 V at No-Load, Room Temperature.

	5 V	**12 V**
Max.	5.00	12.81
Min.	4.89	11.18

8.7.7 5 V Load Change with Full Load on 12 V (uVCC = 3.3 V / 0 A)

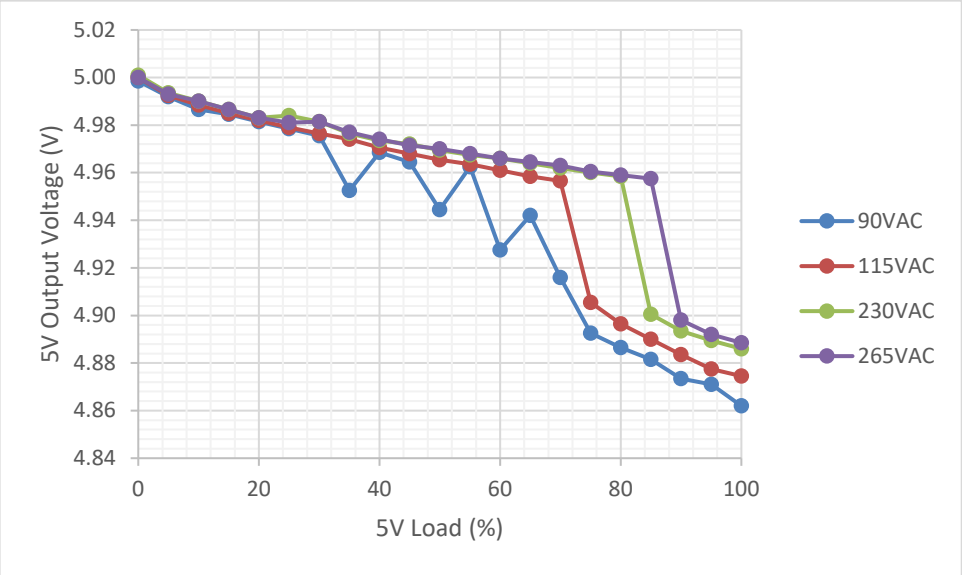


Figure 47 – 5 V Output Voltage while 5 V Output Load Change, 12 V at Full Load, Room Temperature.

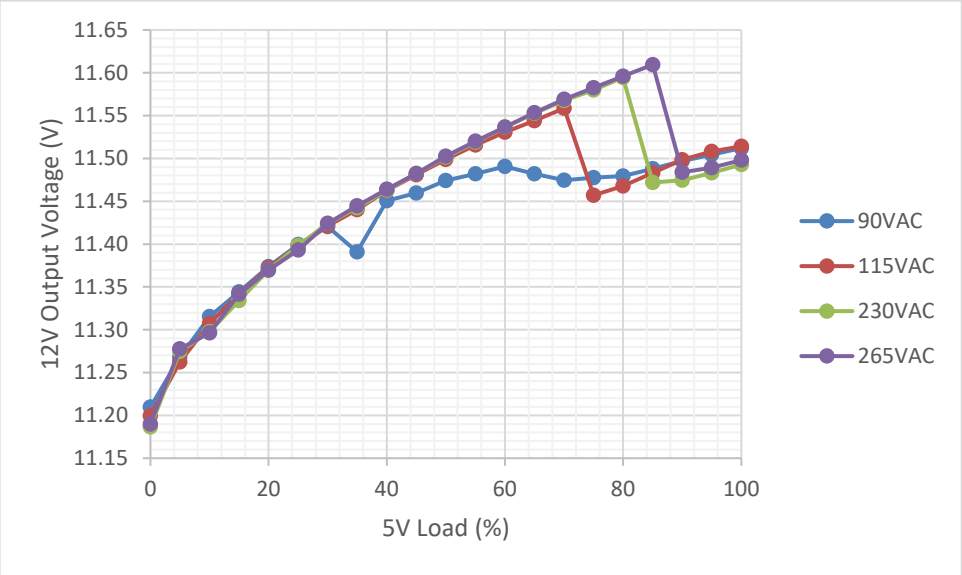


Figure 48 – 12 V Output Voltage while 5 V Output Load Change, 5 V at Full Load, Room Temperature.

	5 V	12 V
Max.	5.00	11.61
Min.	4.87	11.19

8.7.8 5 V Load Change with No-Load on 12 V (uVCC = 3.3 V / 0 A)

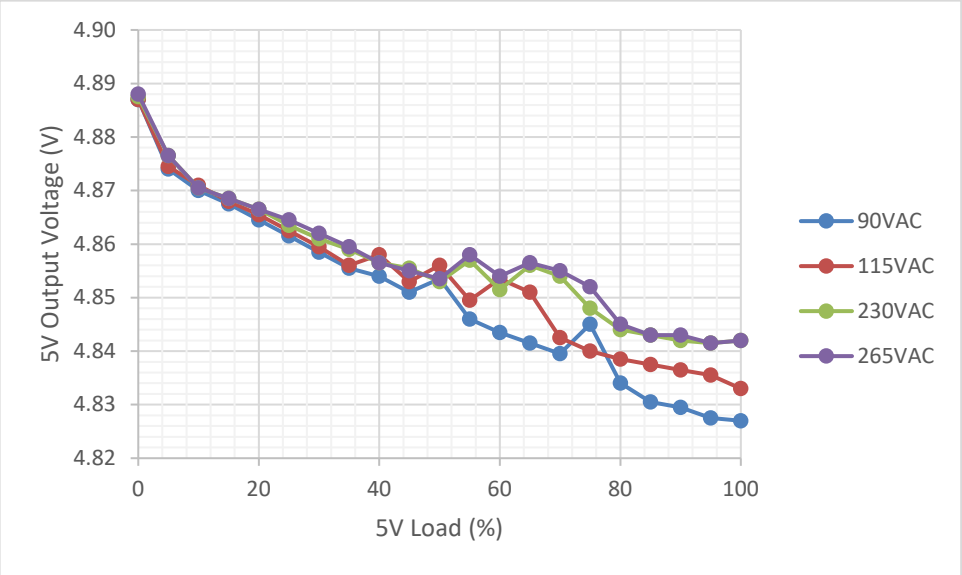


Figure 49 – 5 V Output Voltage while 5 V Output Load Change, 5 V at No-Load, Room Temperature.

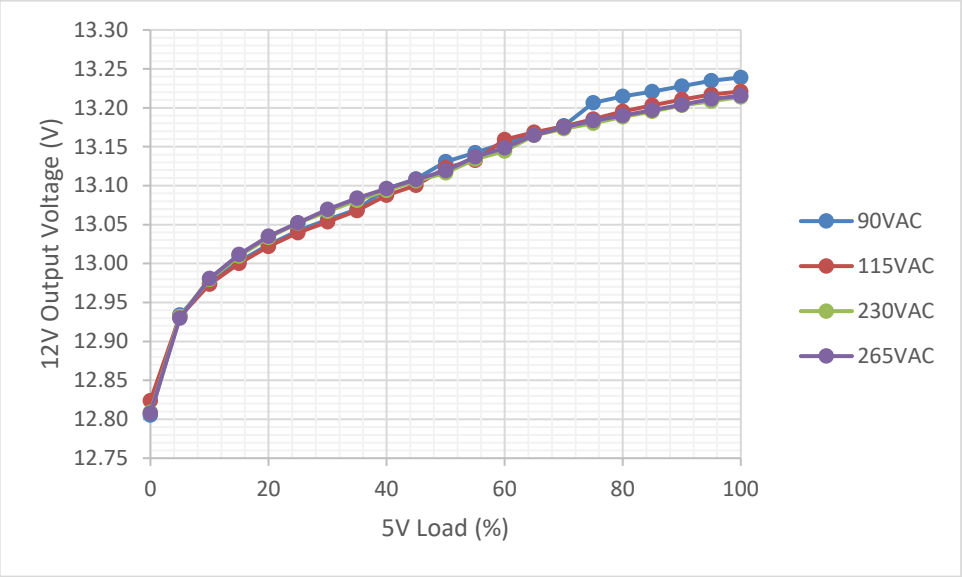


Figure 50 – 12 V Output Voltage while 5 V Output Load Change, 5 V at No-Load, Room Temperature.

	5 V	**12 V**
Max	4.89	13.24
Min	4.83	12.81

9 Thermal Performance

Note: Tested using an IR Camera.

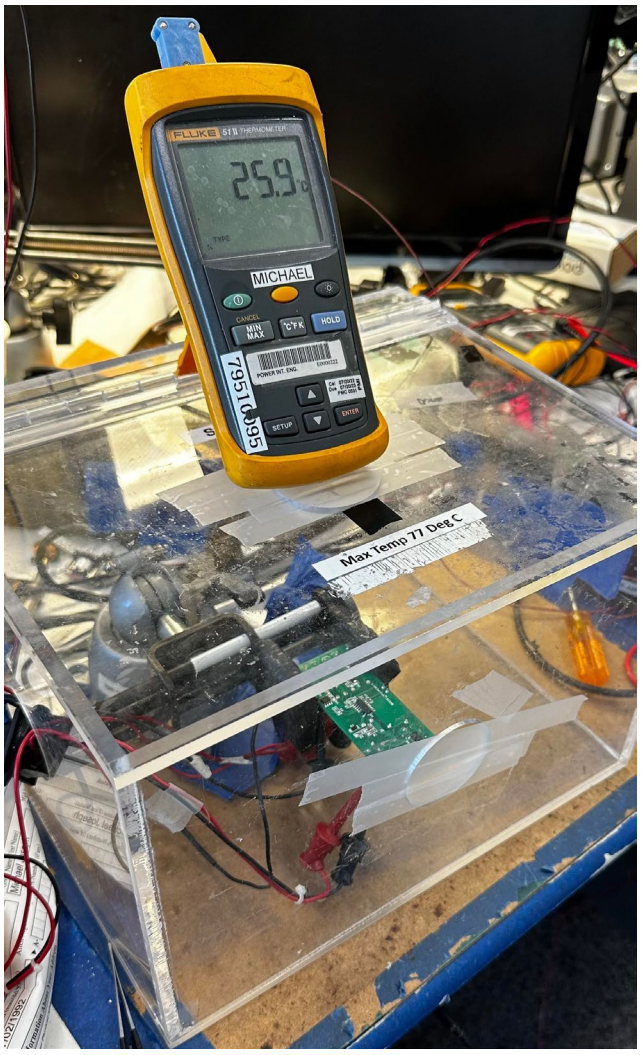


Figure 51 – Test Set-up.

9.1 *90 VAC Input, 5 V / 1.4 A & 12 V / 0.42 A Output (uVCC = 3.3 V / 20 mA)*

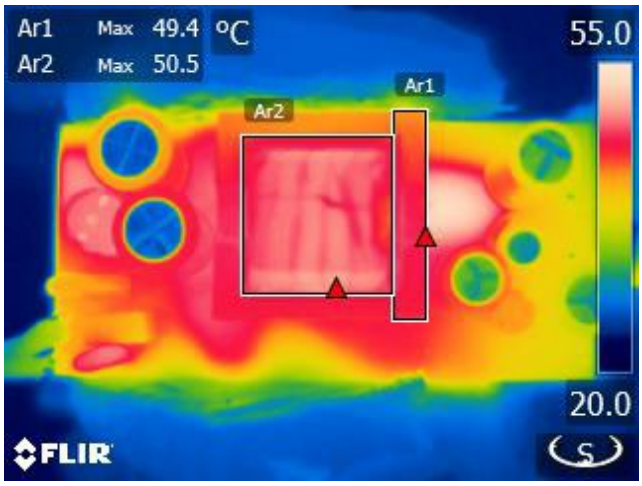


Figure 52 – Transformer Side. 90 VAC, Full Load.

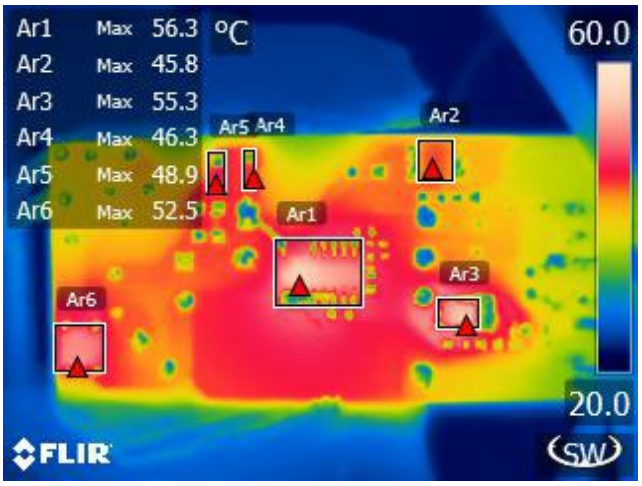


Figure 53 – LinkSwitch-XT2SR Side. 90 VAC, Full Load.

	Reference	°C
Ambient		23.8
Transformer Core (T1)	Ar1	49.4
Transformer Winding (T1)	Ar2	50.4

	Reference	°C
Ambient		23.8
LinkSwitch-XT2SR (U1)	Ar1	56.3
SR FET (Q1)	Ar2	45.8
Schottky (D2)	Ar3	55.3
Snubber Diode (D1)	Ar4	46.3
Snubber Resistor (R2)	Ar5	48.9
Bridge Diode (BR1)	Ar6	52.5

9.2 *265 VAC Input, 5 V / 1.4 A & 12 V / 0.42 A Output (uVCC = 3.3 V / 20 mA)*

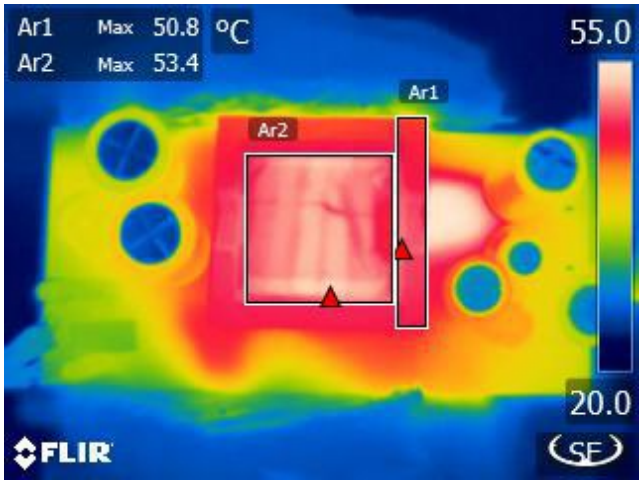


Figure 54 – Transformer Side. 265 VAC, Full Load.

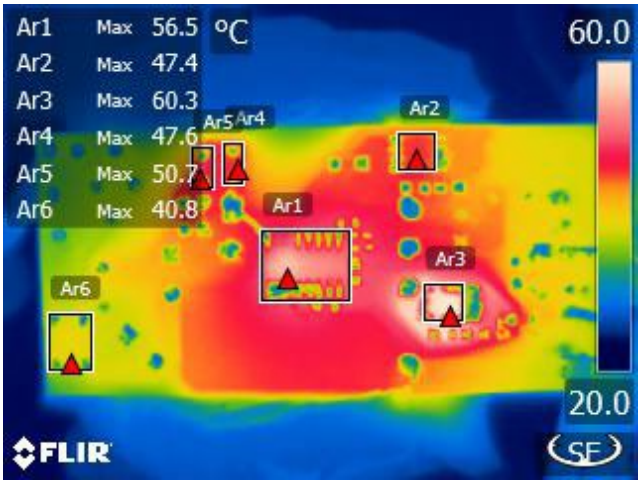


Figure 55 – LinkSwitch-XT2SR Side. 265 VAC, Full Load.

	Reference	°C
Ambient		25
Transformer Core (T1)	Ar1	50.8
Transformer Winding (T1)	Ar2	53.4

	Reference	°C
Ambient		25
LinkSwitch (U1)	Ar1	56.5
SR FET (Q1)	Ar2	47.4
Schottky (D2)	Ar3	60.3
Snubber Diode (D1)	Ar4	47.6
Snubber Resistor (R2)	Ar5	50.7
Bridge Diode (BR1)	Ar6	40.8

10 Thermal Performance at 50 °C Ambient

Note: A thermal chamber is used to increase the ambient temperature up to 50 °C. Unit is placed inside a box to prevent air flow. Soak for 1 hour.

Figure 56 – Thermal Chamber Test Set-up.

10.1 *90 VAC Input, 5 V / 1.4 A & 12 V / 0.42 A Output (uVCC = 3.3 V / 20 mA)*

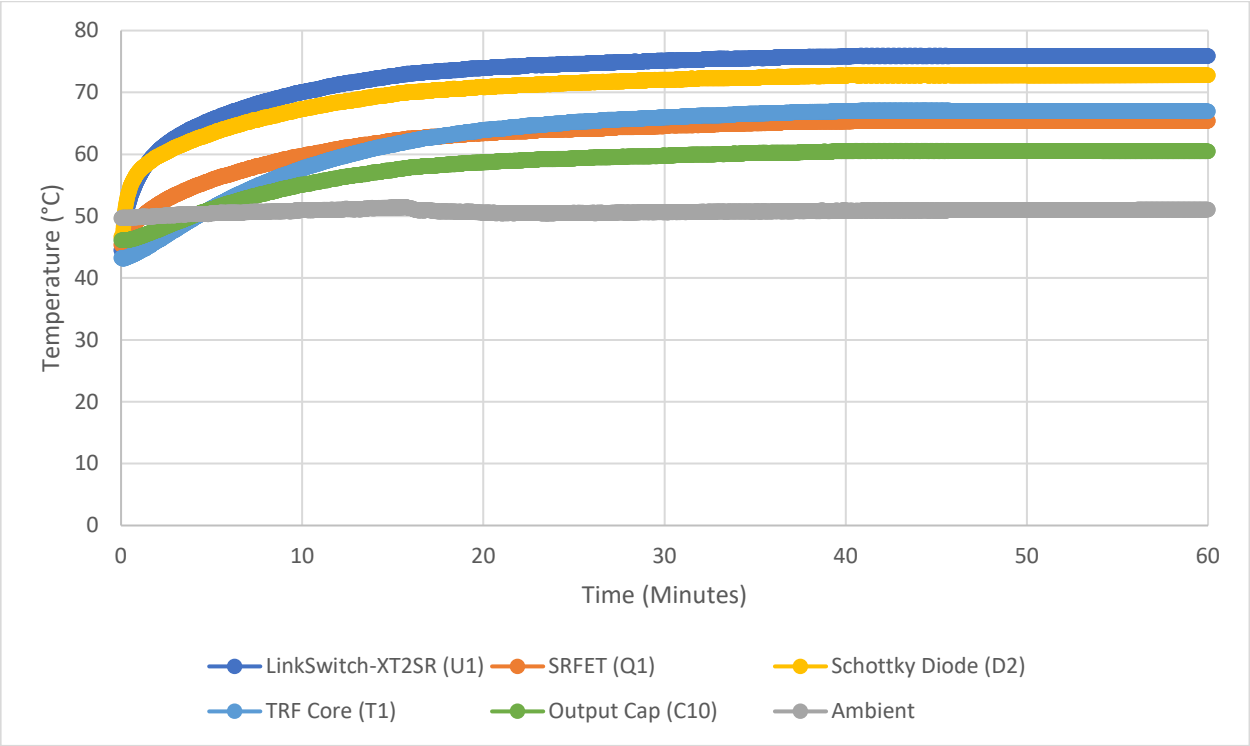


Figure 57 – Thermal Profile at 90 VAC Input, Ambient = 50 °C.

	Maximum Temperature ºC
Ambient	51.5
LinkSwitch-XT2SR (U1)	76
SRFET (Q1)	65.4
Schottky Diode (D2)	72.8
TRF Core (T1)	67.3
5 V COUT (C10)	60.6

10.2 *265 VAC Input, 5 V / 1.4 A & 12 V / 0.42 A Output (uVCC = 3.3 V / 20 mA)*

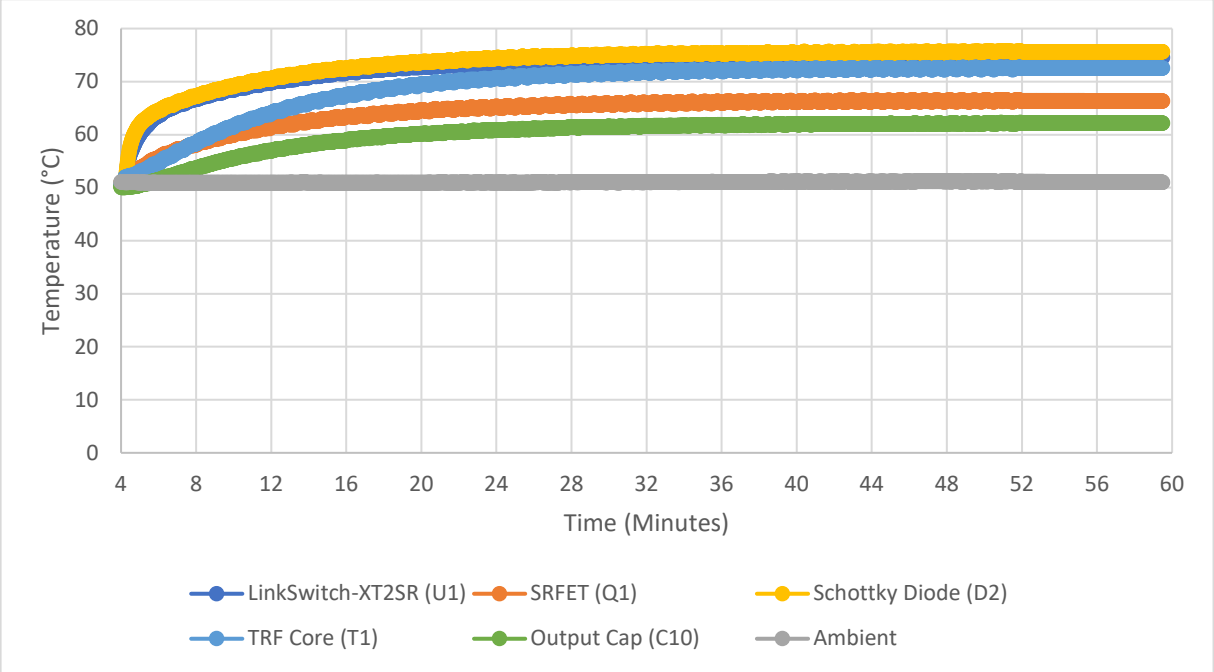


Figure 58 – Thermal Profile at 265 VAC Input, Ambient = 50 °C.

	Maximum Temperature ºC
Ambient	51.8
LinkSwitch-XT2SR (U1)	74.8
SRFET (Q1)	66.7
Schottky Diode (D2)	75.9
TRF Core (T1)	72.8
5 V C_{OUT} (C10)	62.3

11 Thermal Shutdown Performance

Note: A thermal chamber is used to increase the ambient temperature until unit goes to thermal shutdown. Unit is placed inside a box to prevent air flow.

11.1 *90 VAC Input, 5 V / 1.4 A & 12 V / 0.42 A Output (uVCC = 3.3 V / 20 mA)*

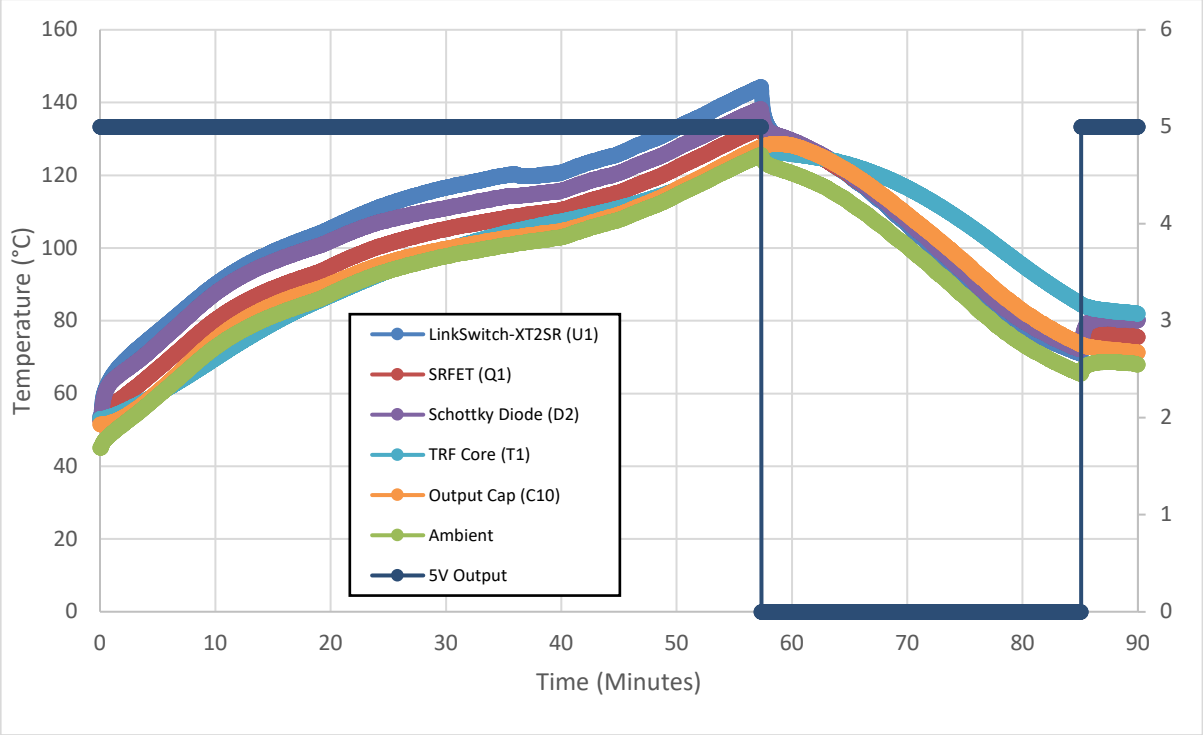


Figure 59 – Thermal Shutdown Performance at 90 VAC Input.

$T_{SHUTDOWN}$ (°C)	$T_{RECOVERY}$ (°C)	$T_{HYSTERESIS}$ (°C)
144.3	71.7	72.6

11.2 *265 VAC Input, 5 V / 1.4 A & 12 V / 0.42 A Output (uVCC = 3.3 V / 20 mA)*

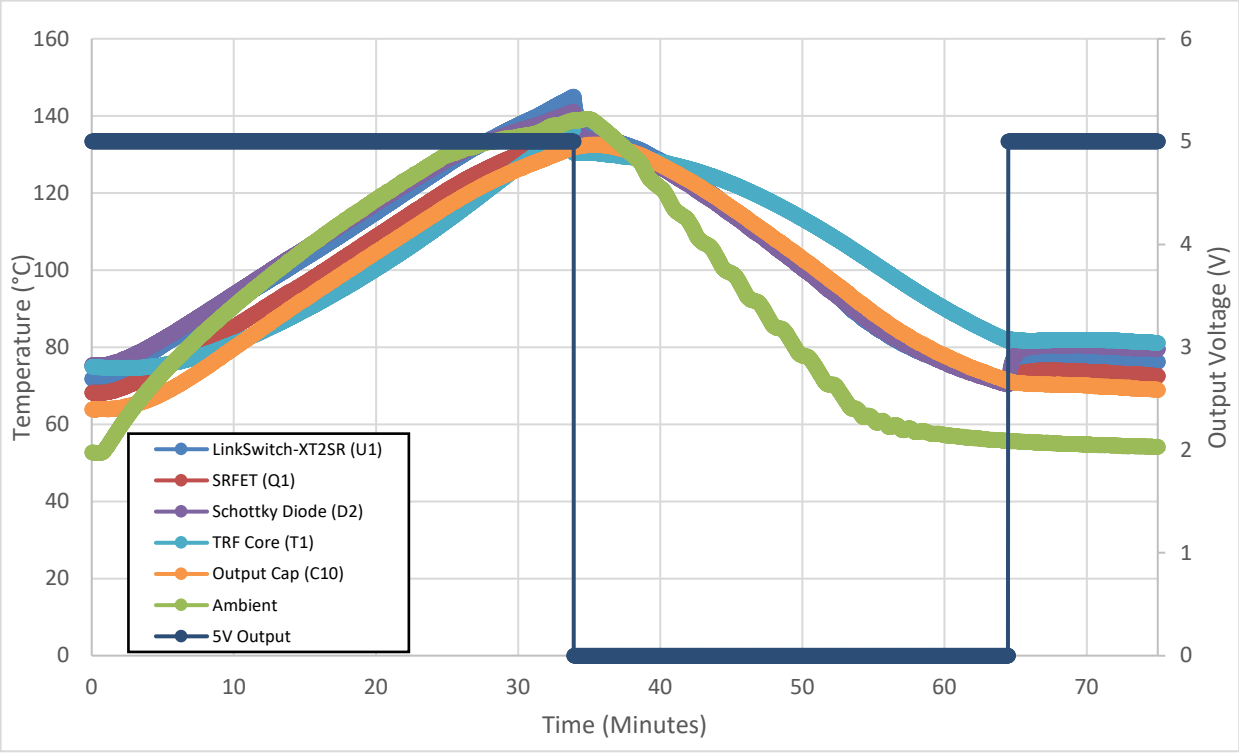


Figure 60 – Thermal Shutdown Performance at 90 VAC Input.

$T_{SHUTDOWN}$ (ºC)	$T_{RECOVERY}$ (ºC)	$T_{HYSTERESIS}$ (ºC)
145	70.8	74.2

12 Waveforms

12.1 *Output Waveforms During Start-up – CC Load (uVCC = 3.3 V / 0 A)*

12.1.1 5 V and 12 V at Full Load Condition

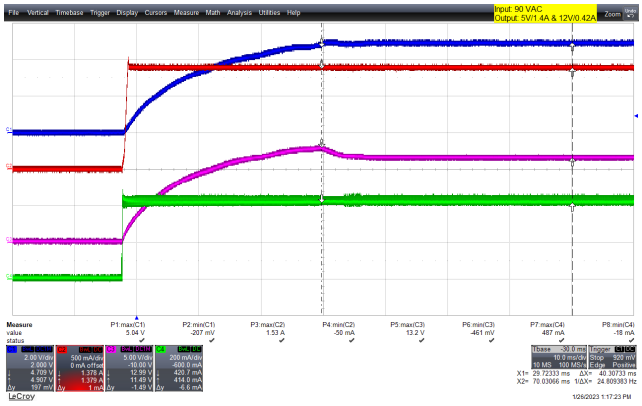


Figure 61 – Output Voltage and Current Waveforms.
90 VAC Input.
Upper: 5 V_{OUT}. 2 V / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
10 ms / div.

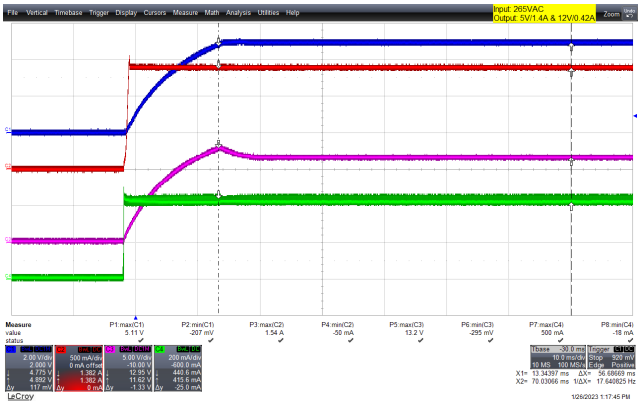


Figure 62 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: 5 V_{OUT}. 2 V / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
10 ms / div.

12.1.2 5 V at No-Load, 12 V at Full Load Condition

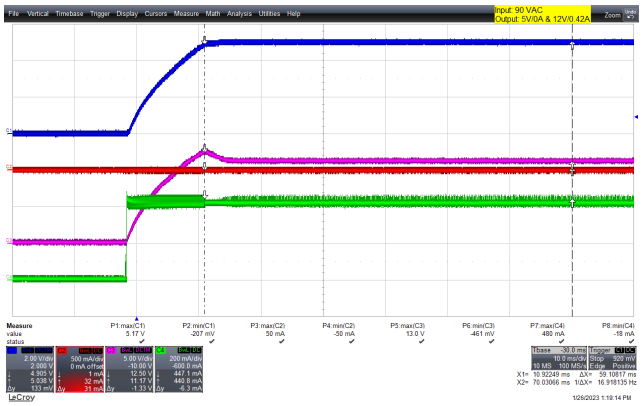


Figure 63 – Output Voltage and Current Waveforms.
90 VAC Input.
Upper: 5 V_{OUT}. 2 V / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
10 ms / div.

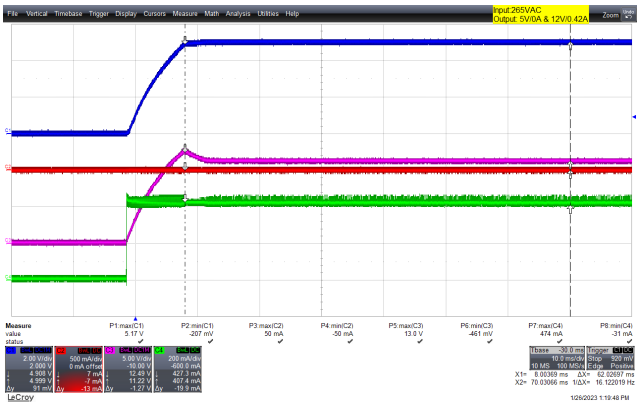


Figure 64 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: 5 V_{OUT}. 2 V / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
10 ms / div.

12.1.3 5 V at Full Load, 12 V at No-Load Condition

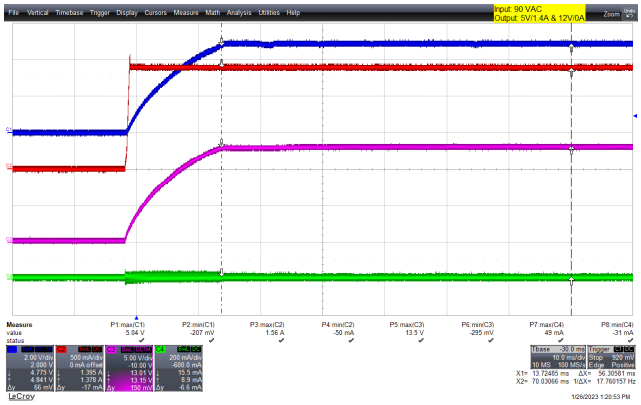


Figure 65 – Output Voltage and Current Waveforms.
90 VAC Input.
Upper: 5 V_{OUT}. 2 V / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
10 ms / div.

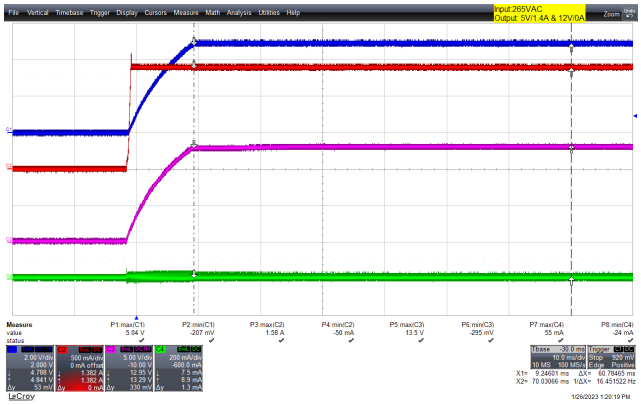


Figure 66 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: 5 V_{OUT}. 2 V / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
10 ms / div.

12.1.4 5 V and 12 V at No-Load Condition

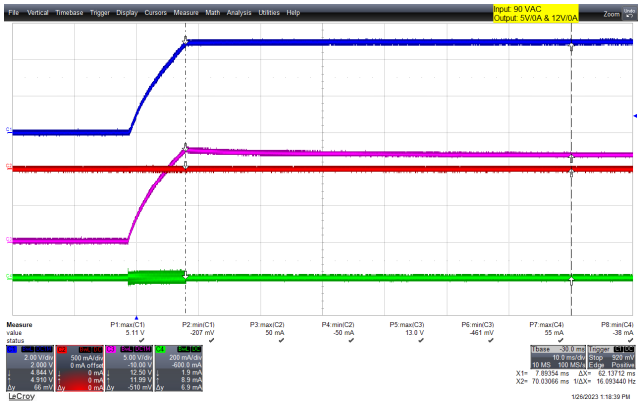


Figure 67 – Output Voltage and Current Waveforms.
90 VAC Input.
Upper: 5 V_{OUT}. 2 V / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
10 ms / div.

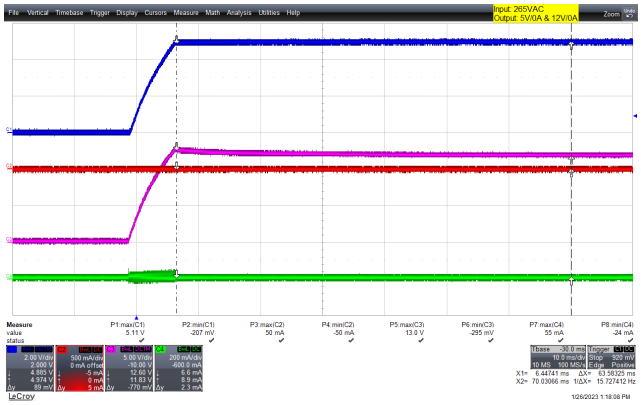


Figure 68 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: 5 V_{OUT}. 2 V / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
10 ms / div.

12.2 *Output Waveforms During Start-up – CC Load (uVCC = 3.3 V / 20 mA)*

12.2.1 5 V and 12 V at Full Load Condition

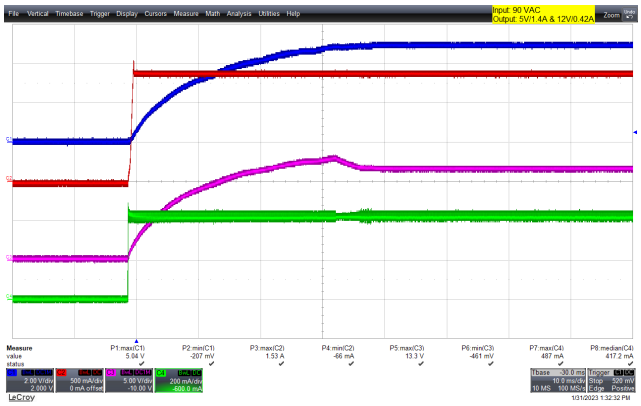


Figure 69 – Output Voltage and Current Waveforms.
90 VAC Input.
Upper: 5 V_{OUT}. 2 V / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
10 ms / div.

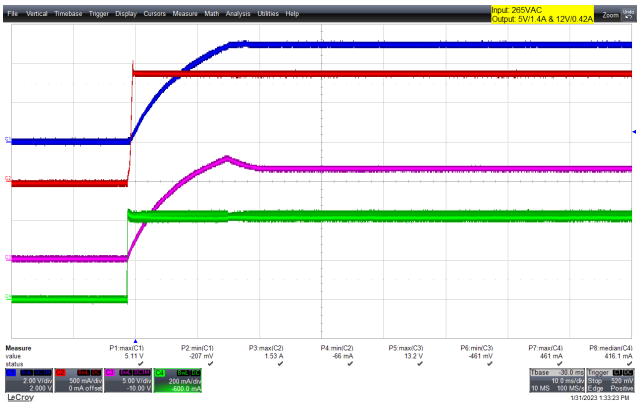


Figure 70 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: 5 V_{OUT}. 2 V / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
10 ms / div.

12.3 *Load Transient Response*

12.3.1 12 V Load Transient – Full-Load at 5 V Output

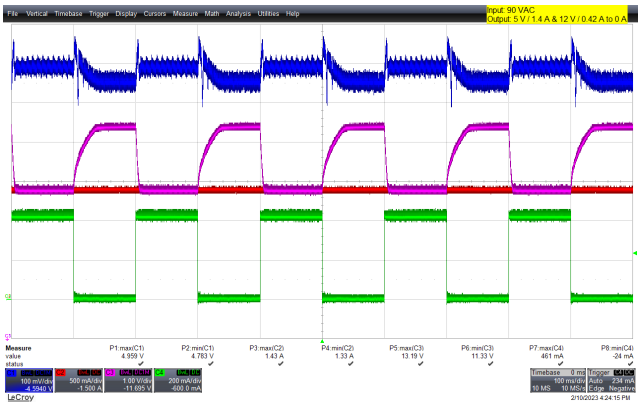


Figure 71 – 0 A – 0.42 A, 12 V Load Step Transient Response, 90 VAC.
5 V_{MAX}: 4.96 V.; 5 V_{MIN}: 4.78 V.
12 V_{MAX}: 13.19 V. 12 V_{MIN}: 11.33 V.
Upper: 5 V_{OUT}. 100 mV / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 1 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
100 ms / div.

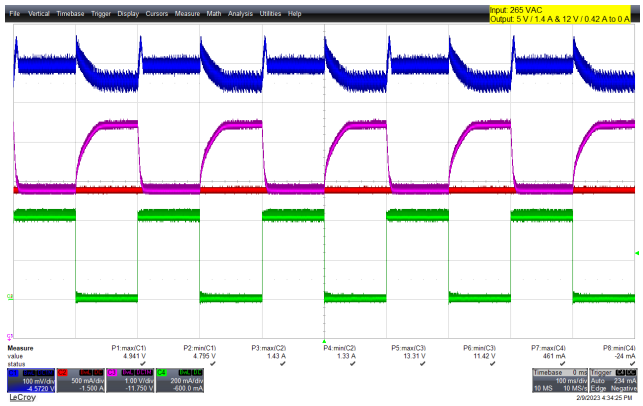


Figure 72 – 0 A – 0.42 A, 12 V Load Step Transient Response. 265 VAC.
5 V_{MAX}: 4.94 V.; 5 V_{MIN}: 4.79 V.
12 V_{MAX}: 13.31 V. 12 V_{MIN}: 11.42 V.
Upper: 5 V_{OUT}. 100 mV / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 1 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
100 ms / div.

12.3.2 12 V Load Transient – No-Load at 5 V Output

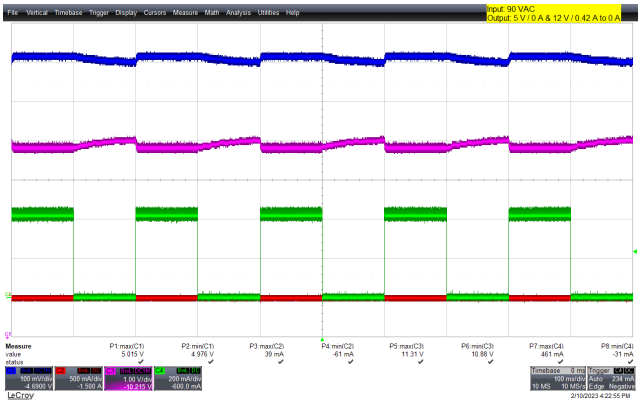


Figure 73 – 0 A – 0.42 A, 12 V Load Step Transient Response, 90 VAC.
5 V_{MAX}: 5.02 V.; 5 V_{MIN}: 4.98 V.
12 V_{MAX}: 11.31 V. 12 V_{MIN}: 10.88 V.
Upper: 5 V_{OUT}. 100 mV / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 1 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
100 ms / div.

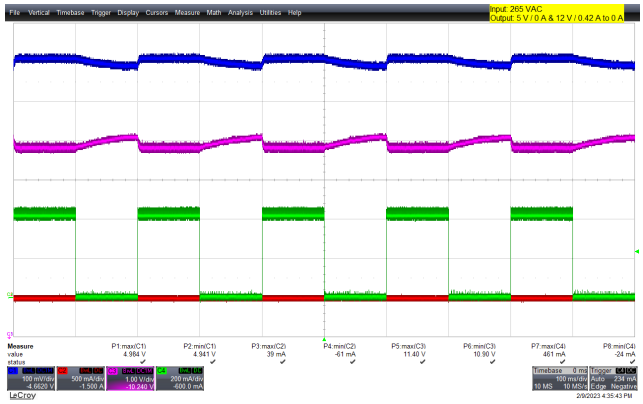


Figure 74 – 0 A – 0.42 A, 12 V Load Step Transient Response. 265 VAC.
5 V_{MAX}: 4.98 V.; 5 V_{MIN}: 4.94 V.
12 V_{MAX}: 11.4 V. 12 V_{MIN}: 10.9 V.
Upper: 5 V_{OUT}. 100 mV / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 1 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
100 ms / div.

12.3.3 5 V Load Transient – Full-Load at 12 V Output

Figure 75 – 0 A – 0.42 A, 5 V Load Step Transient Response, 90 VAC.
5 V_{MAX}: 5.01 V.; 5 V_{MIN}: 4.81 V.
12 V_{MAX}: 11.62 V. 12 V_{MIN}: 10.89 V.
Upper: 5 V_{OUT}. 100 mV / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 1 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
100 ms / div.

Figure 76 – 0 A – 0.42 A, 5 V Load Step Transient Response. 265 VAC.
5 V_{MAX}: 4.98 V.; 5 V_{MIN}: 4.80 V.
12 V_{MAX}: 11.70 V. 12 V_{MIN}: 10.9 V.
Upper: 5 V_{OUT}. 100 mV / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 1 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
100 ms / div.

12.3.4 5 V Load Transient – No-Load at 12 V Output

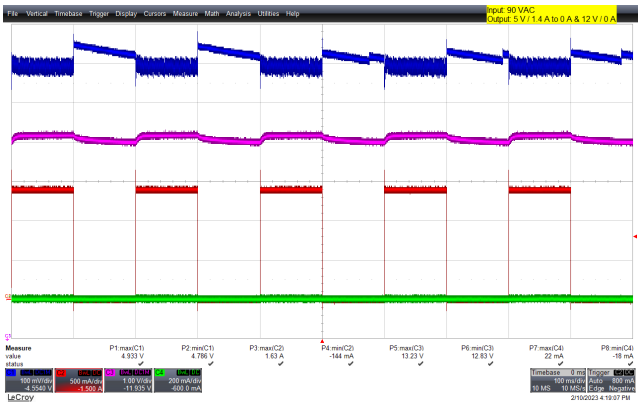


Figure 77 – 0 A – 0.42 A, 5 V Load Step Transient Response, 90 VAC.
5 V_{MAX}: 4.93 V.; 5 V_{MIN}: 4.79 V.
12 V_{MAX}: 13.23 V. 12 V_{MIN}: 12.83 V.
Upper: 5 V_{OUT}. 100 mV / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 1 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
100 ms / div.

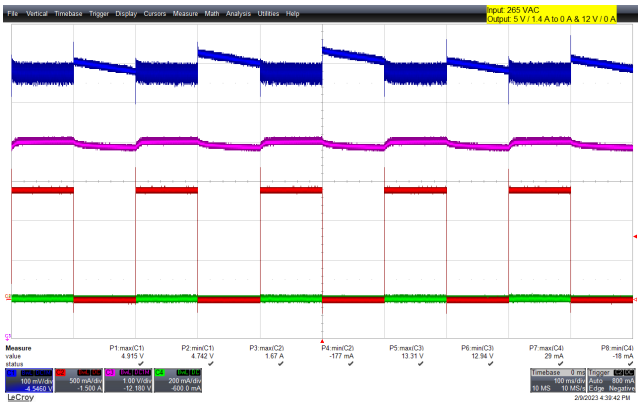


Figure 78 – 0 A – 0.42 A, 5 V Load Step Transient Response. 265 VAC.
5 V_{MAX}: 4.92 V.; 5 V_{MIN}: 4.74 V.
12 V_{MAX}: 13.31 V. 12 V_{MIN}: 12.94 V.
Upper: 5 V_{OUT}. 100 mV / div.
Upper Middle: 5 I_{OUT}, 500 mA / div.
Lower Middle: 12 V_{OUT}, 1 V / div.
Lower: 12 I_{OUT}, 200 mA / div.
100 ms / div.

12.4 *Switching Waveforms*

12.4.1 LinkSwitch-XT2SR Waveforms During Normal Operation

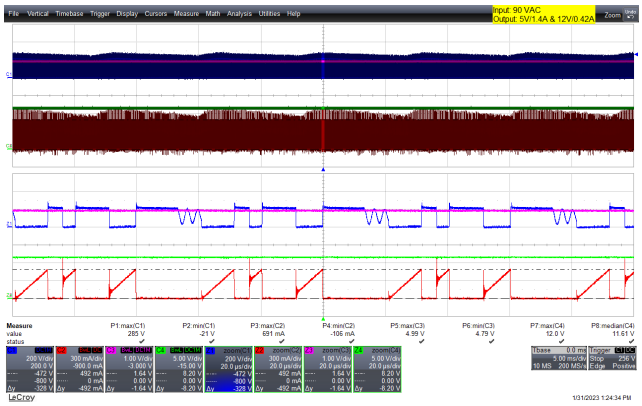


Figure 79 – Drain Voltage and Current Waveforms.
90 VAC Input, Full Load.
Upper: LNK-XT2SR_V_{DS}. 200 V / div.
Upper Middle: 5 V_{OUT}, 1 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 300 mA / div.
5 ms / div.
Zoom: 20 µs / div.

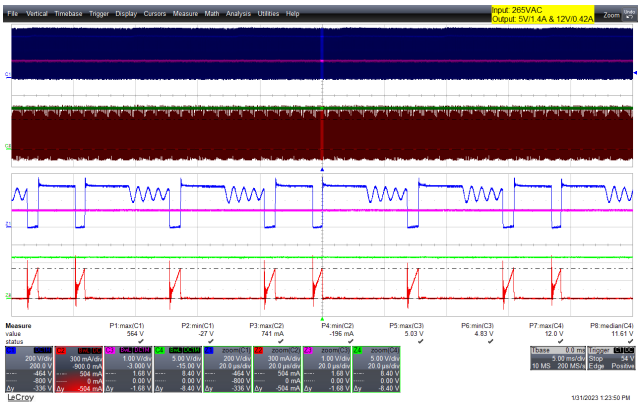


Figure 80 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (564 V_{MAX}).
Upper: LNK-XT2SR_V_{DS}. 200 V / div.
Upper Middle: 5 V_{OUT}, 1 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 300 mA / div.
5 ms / div.
Zoom: 20 µs / div.

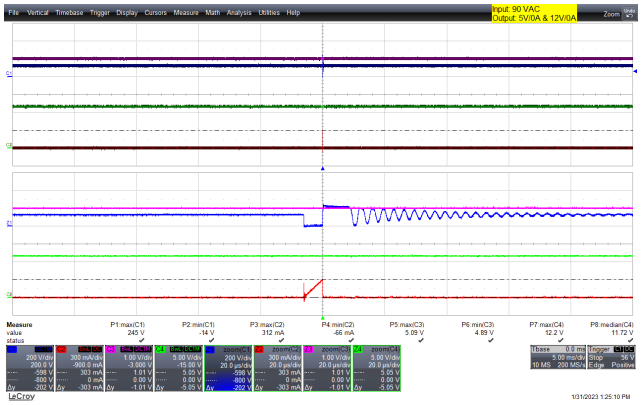


Figure 81 – Drain Voltage and Current Waveforms.
90 VAC Input, No-Load.
Upper: LNK-XT2SR_V_{DS}. 200 V / div.
Upper Middle: 5 V_{OUT}, 1 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 300 mA / div.
5 ms / div.
Zoom: 20 µs / div.

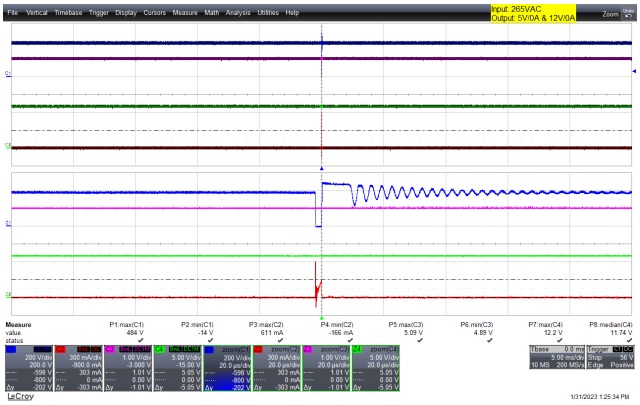


Figure 82 – Drain Voltage and Current Waveforms.
265 VAC Input, No-Load, (484 V_{MAX}).
Upper: LNK-XT2SR_V_{DS}. 200 V / div.
Upper Middle: 5 V_{OUT}, 1 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 300 mA / div.
5 ms / div.
Zoom: 20 µs / div.

12.4.2 LinkSwitch-XT2SR Waveforms During Start-up

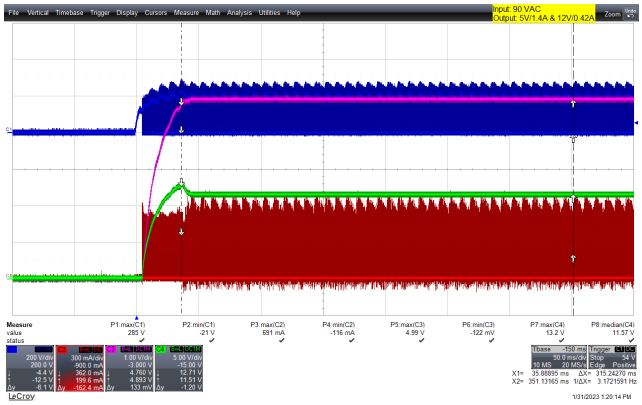


Figure 83 – Drain Voltage and Current Waveforms.
90 VAC Input, Full Load.
Upper: LNK-XT2SR_V_{DS}. 200 V / div.
Upper Middle: 5 V_{OUT}, 1 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 300 mA / div.
50 ms / div.

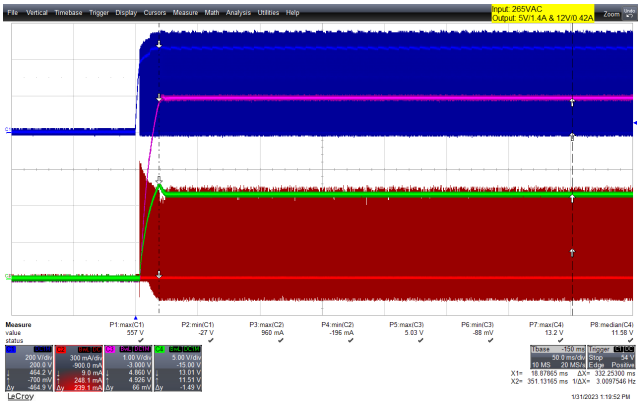


Figure 84 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (557 V_{MAX}).
Upper: LNK-XT2SR_VDS. 200 V / div.
Upper Middle: 5 V_{OUT}, 1 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_IDS, 300 mA / div.
5 ms / div.

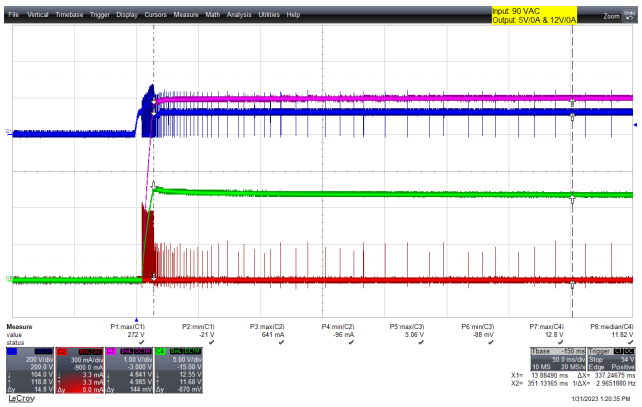


Figure 85 – Drain Voltage and Current Waveforms.
90 VAC Input, No-Load.
Upper: LNK-XT2SR_VDS. 200 V / div.
Upper Middle: 5 V_{OUT}, 1 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_IDS, 300 mA / div.
5 ms / div.

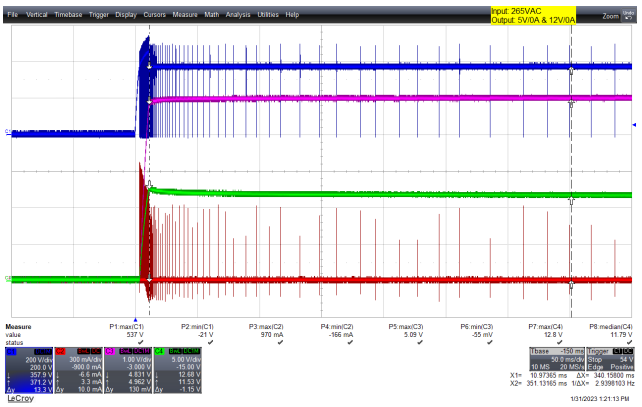


Figure 86 – Drain Voltage and Current Waveforms.
265 VAC Input, No-Load, (537 V_{MAX}).
Upper: LNK-XT2SR_VDS. 200 V / div.
Upper Middle: 5 V_{OUT}, 1 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_IDS, 300 mA / div.
5 ms / div.

12.4.3 SRFET Waveforms During Normal Operation

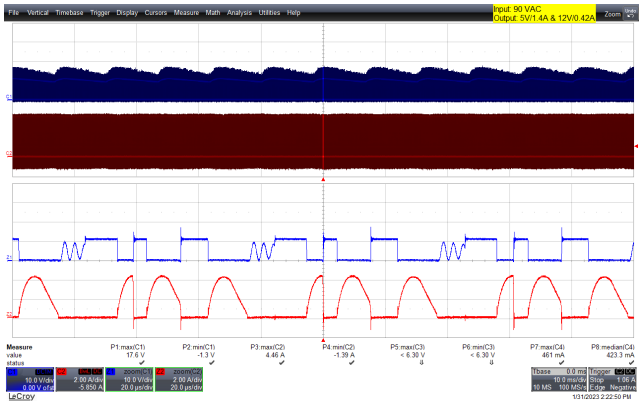


Figure 87 – 5 V SRFET Voltage Waveforms.
90 VAC Input, Full Load.
Upper: SRFET_V_{DS}. 10 V / div.
Lower: SRFET_I_{DS}, 2 A / div.
10 ms / div.
Zoom: 20 μs / div.

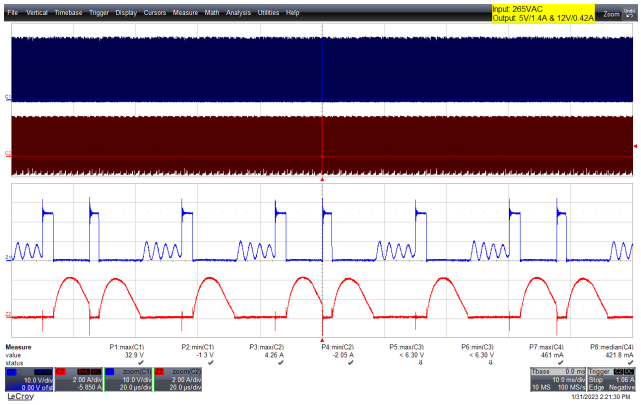


Figure 88 – 5 V SRFET Voltage Waveforms.
265 VAC Input, Full Load (32.9 V_{MAX}).
Upper: SRFET_V_{DS}. 10 V / div.
Lower: SRFET_I_{DS}, 2 A / div.
10 ms / div.
Zoom: 20 μs / div.

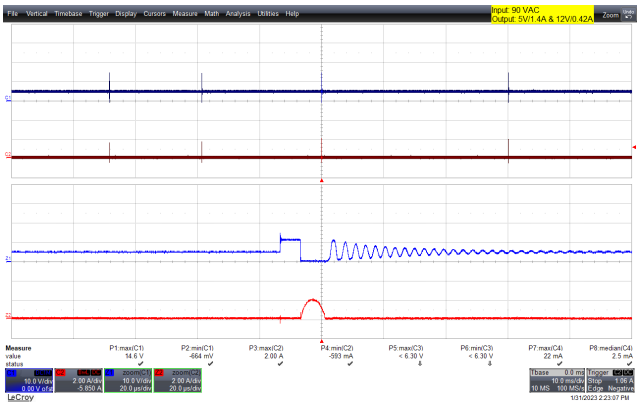


Figure 89 – 5 V SRFET Voltage Waveforms.
90 VAC Input, No-Load.
Upper: SRFET_V_{DS}. 10 V / div.
Lower: SRFET_I_{DS}, 2 A / div.
10 ms / div.
Zoom: 20 μs / div.

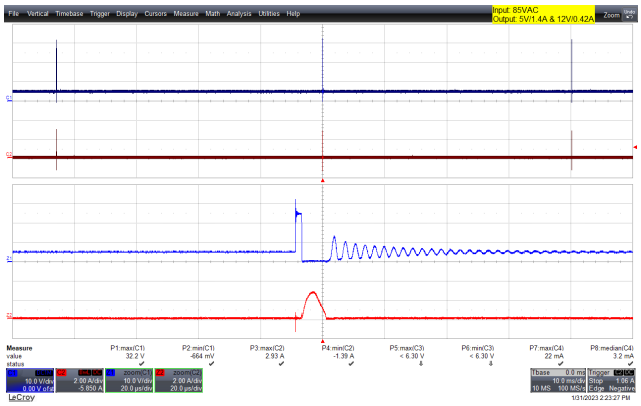


Figure 90 – 5 V SRFET Voltage Waveforms.
265 VAC Input, No-Load (32.2 V_{MAX}).
Upper: SRFET_V_{DS}. 10 V / div.
Lower: SRFET_I_{DS}, 2 A / div.
10 ms / div.
Zoom: 20 μs / div.

12.4.4 SRFET Waveforms During Start-up

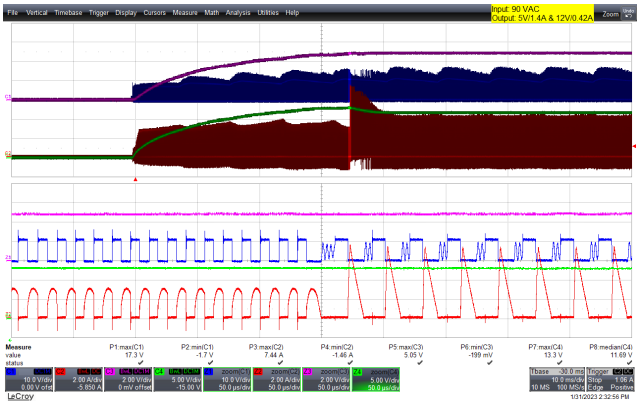


Figure 91 – 5 V SRFET Voltage Waveforms.
90 VAC Input, Full Load.
Upper: 5 V_{OUT}, 2 V / div.
Upper Middle: SRFET_V_{DS}. 10 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: SRFET_I_{DS}, 2 A / div.
10 ms / div.
Zoom: 50 µs / div.

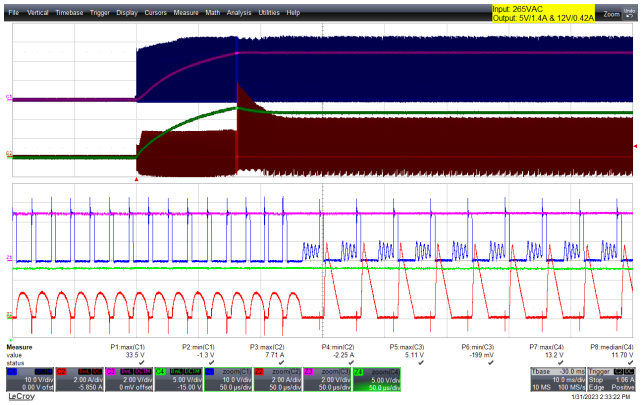


Figure 92 – 5 V SRFET Voltage Waveforms.
265 VAC Input, Full Load (33.5 V_{MAX}).
Upper: 5 V_{OUT}, 2 V / div.
Upper Middle: SRFET_V_{DS}. 10 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: SRFET_I_{DS}, 2 A / div.
10 ms / div.
Zoom: 50 µs / div.

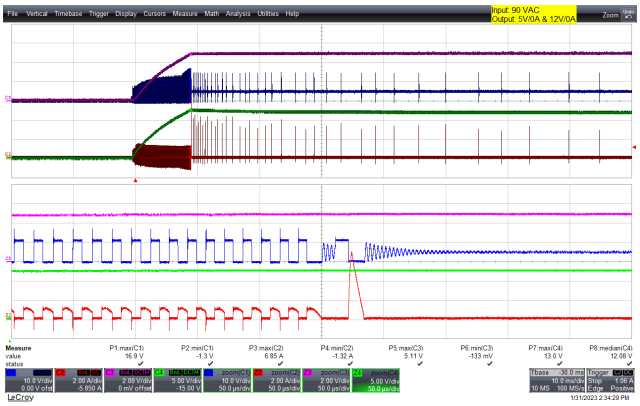


Figure 93 – 5 V SRFET Voltage Waveforms.
90 VAC Input, No-Load.
Upper: 5 V_{OUT}, 2 V / div.
Upper Middle: SRFET_V_{DS}. 10 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: SRFET_I_{DS}, 2 A / div.
10 ms / div.
Zoom: 50 µs / div.

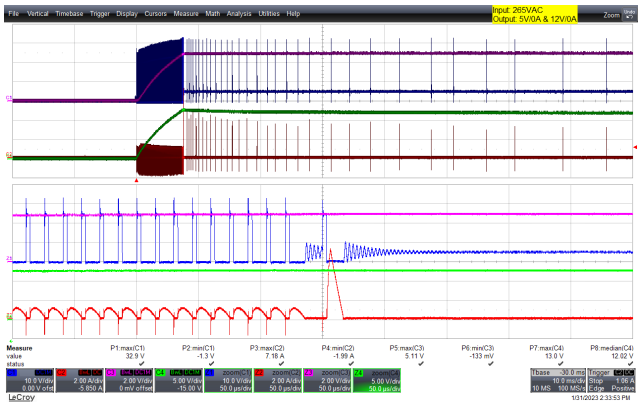


Figure 94 – 5 V SRFET Voltage Waveforms.
265 VAC Input, No-Load (32.9 V_{MAX}).
Upper: 5 V_{OUT}, 2 V / div.
Upper Middle: SRFET_V_{DS}. 10 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: SRFET_I_{DS}, 2 A / div.
10 ms / div.
Zoom: 50 µs / div.

12.4.5 Schottky Diode Waveforms During Normal Operation

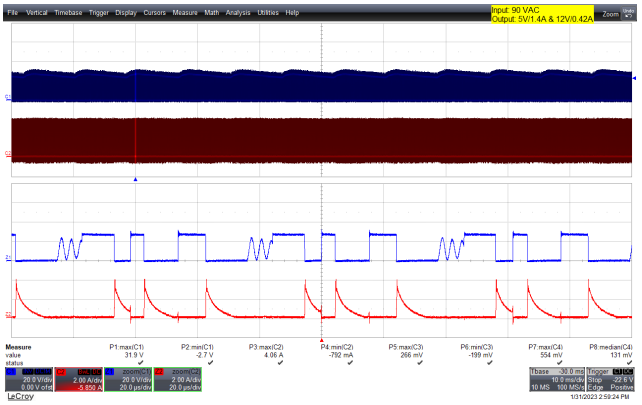


Figure 95 – 12 V Schottky Diode Voltage Waveforms.
90 VAC Input, Full Load.
Upper: Schottky_V_{AK}. 20 V / div.
Lower: Schottky_I_{AK}, 2 A / div.
10 ms / div.
Zoom: 20 μs / div.

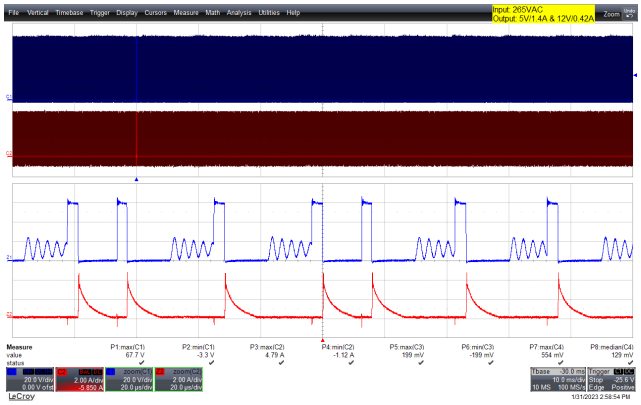


Figure 96 – 12 V Schottky Diode Voltage Waveforms.
265 VAC Input, Full Load (67.7 V_{MAX}).
Upper: Schottky_V_{AK}. 20 V / div.
Lower: Schottky_I_{AK}, 2 A / div.
10 ms / div.
Zoom: 20 μs / div.

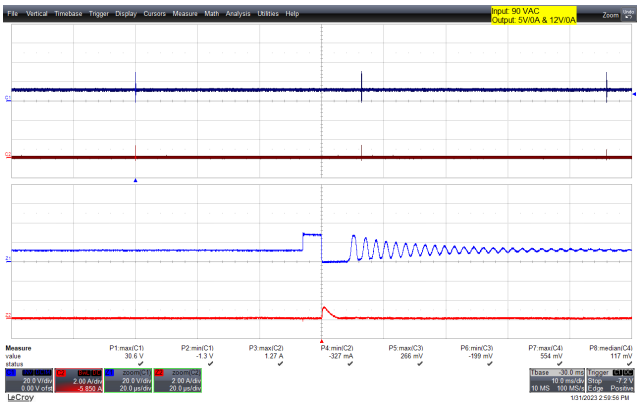


Figure 97 – 12 V Schottky Diode Voltage Waveforms.
90 VAC Input, No-Load.
Upper: Schottky_V_{AK}. 20 V / div.
Lower: Schottky_I_{AK}, 2 A / div.
10 ms / div.
Zoom: 20 μs / div.

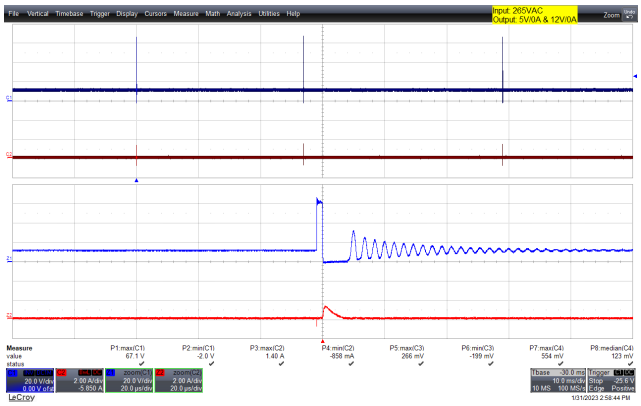


Figure 98 – 12 V Schottky Diode Voltage Waveforms.
265 VAC Input, No-Load (67.1 V_{MAX}).
Upper: Schottky_V_{AK}. 20 V / div.
Lower: Schottky_I_{AK}, 2 A / div.
10 ms / div.
Zoom: 20 μs / div.

12.4.6 Schottky Diode Waveforms During Start-up

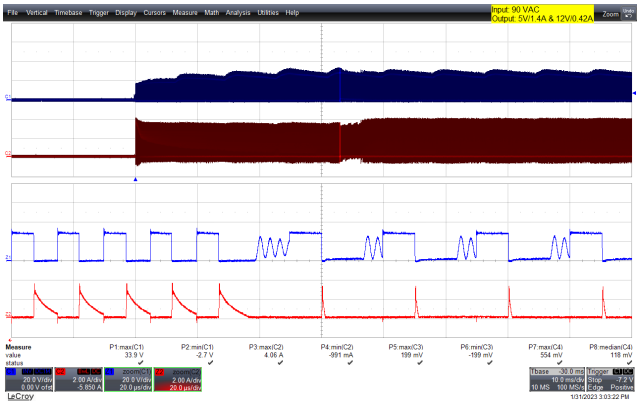


Figure 99 – 12 V Schottky Diode Voltage Waveforms.
90 VAC Input, Full Load.
Upper: Schottky_V_{AK}. 20 V / div.
Lower: Schottky_I_{AK}, 2 A / div.
10 ms / div.
Zoom: 20 µs / div.

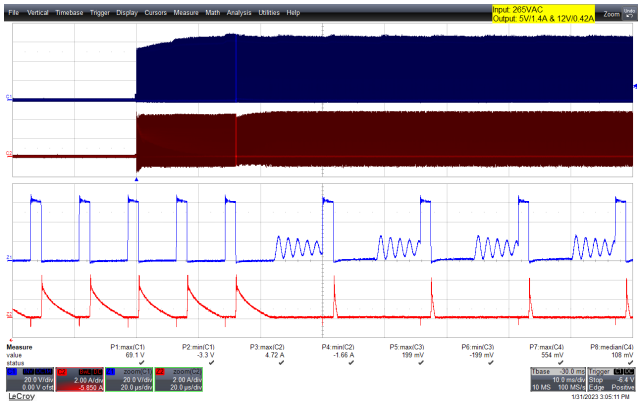


Figure 100 – 12 V Schottky Diode Voltage Waveforms.
265 VAC Input, Full Load (69.1 V_{MAX}).
Upper: Schottky_V_{AK}. 20 V / div.
Lower: Schottky_I_{AK}, 2 A / div.
10 ms / div.
Zoom: 20 µs / div.

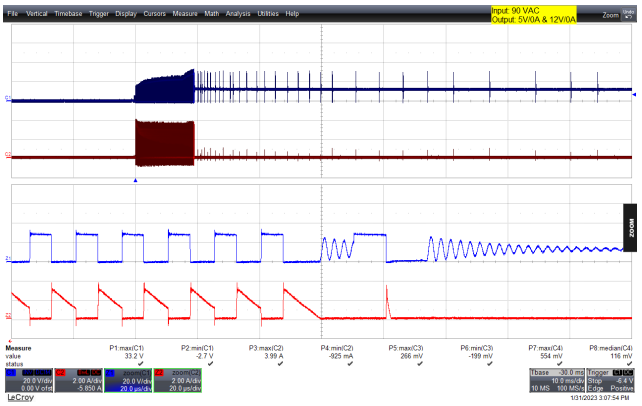


Figure 101 – 12 V Schottky Diode Voltage Waveforms.
90 VAC Input, No-Load.
Upper: Schottky_V_{AK}. 20 V / div.
Lower: Schottky_I_{AK}, 2 A / div.
10 ms / div.
Zoom: 20 µs / div.

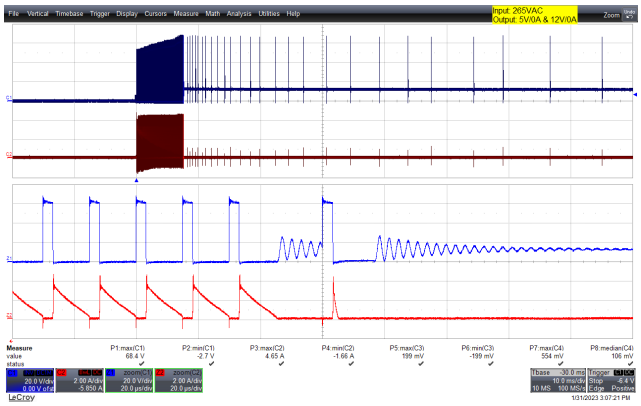


Figure 102 – 12 V Schottky Diode Voltage Waveforms.
265 VAC Input, No-Load (68.4 V_{MAX}).
Upper: Schottky_V_{AK}. 20 V / div.
Lower: Schottky_I_{AK}, 2 A / div.
10 ms / div.
Zoom: 20 µs / div.

12.4.7 Output Voltage and Current Waveform with 5 V Output Shorted

Figure 103 – Output Voltage and Current Waveforms.
90 VAC Input. Output Shorted.
Upper: LNK-XT2SR_V_{DS}. 200 V / div.
Upper Middle: 5 V_{OUT}, 1 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 500 mA / div.
500 ms / div.
Zoom: 50 ms / div.

Figure 104 – Output Voltage and Current Waveforms.
265 VAC Input. Output Shorted.
Upper: LNK-XT2SR_V_{DS}. 200 V / div.
Upper Middle: 5 V_{OUT}, 1 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 500 mA / div.
500 ms / div.
Zoom: 50 ms / div.

12.4.8 Output Voltage and Current Waveform with 12 V Output Shorted

Figure 105 – Output Voltage and Current Waveforms.
90 VAC Input. Output Shorted.
Upper: LNK-XT2SR_V_{DS}. 200 V / div.
Upper Middle: 5 V_{OUT}, 1 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 500 mA / div.
500 ms / div.
Zoom: 50 ms / div.

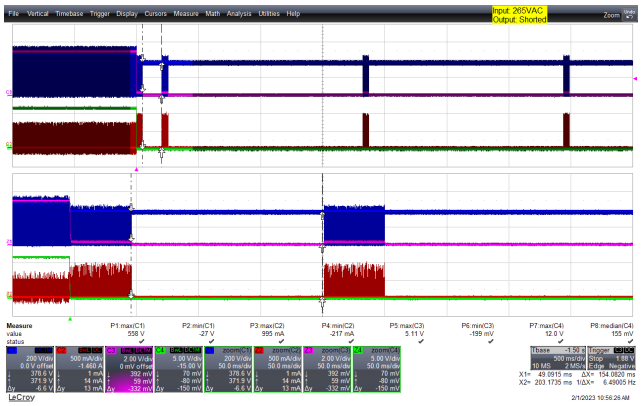


Figure 106 – Output Voltage and Current Waveforms.
265 VAC Input. Output Shorted.
Upper: LNK-XT2SR_V_{DS}. 200 V / div.
Upper Middle: 5 V_{OUT}, 1 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 500 mA / div.
500 ms / div.
Zoom: 50 ms / div.

12.5 *Output Ripple Measurements*

12.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

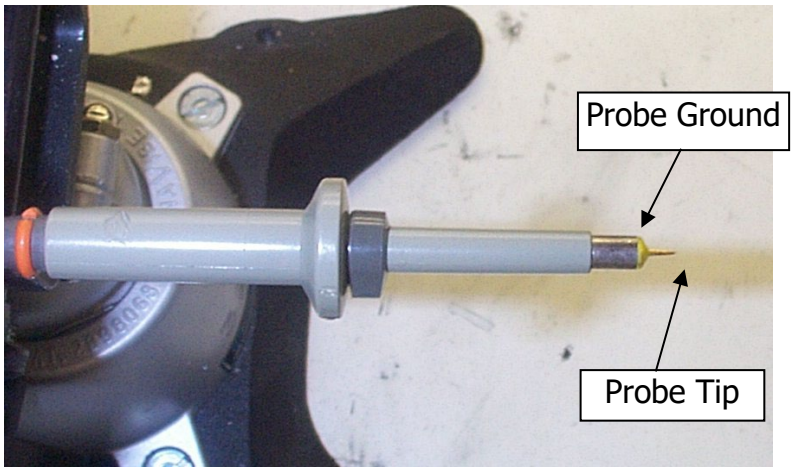


Figure 107 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

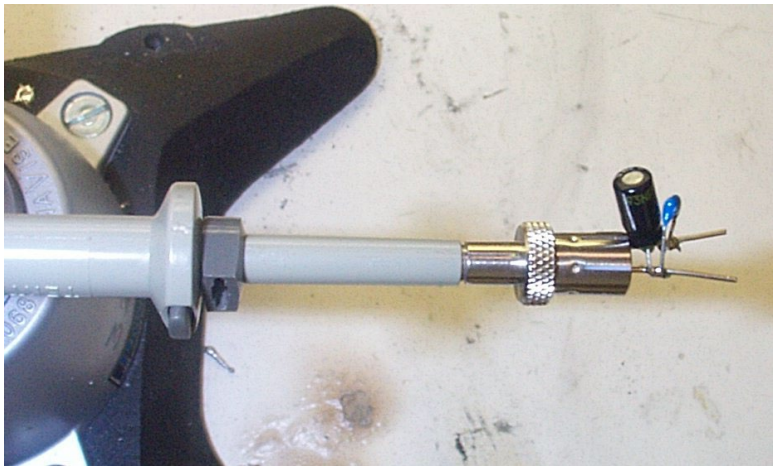


Figure 108 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

12.5.2 Ripple Voltage Waveforms (uVCC = 3.3 V / 0 A)

Note: Both 5 V & 12 V output are loaded with the same percentage.

12.5.2.1 0% Load

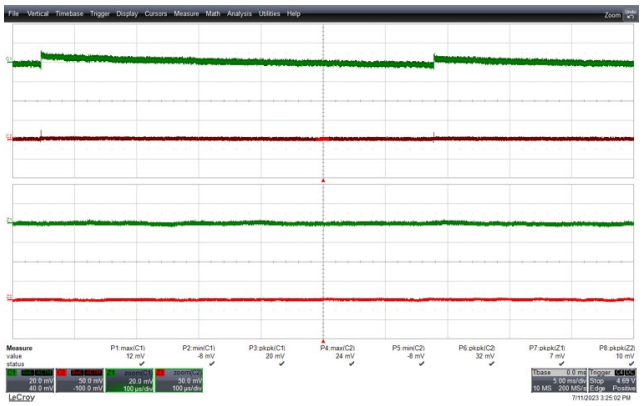


Figure 109 – Output Ripple Voltage Waveforms.
90 VAC Input.
5 V_{PK-PK}: 20 mV, 12 V_{PK-PK}: 32 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

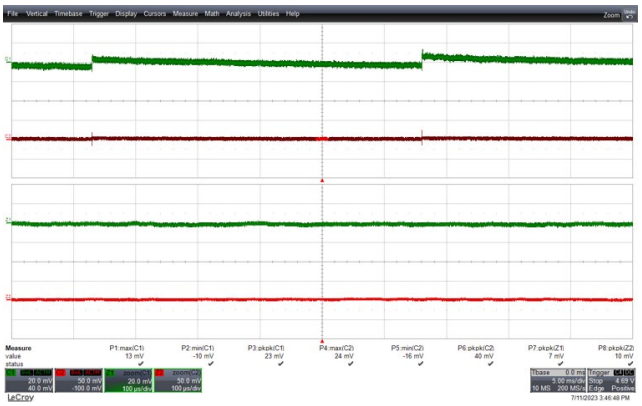


Figure 110 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
5 V_{PK-PK}: 20 mV, 12 V_{PK-PK}: 32 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

12.5.2.2 25% Load

Figure 111 – Output Ripple Voltage Waveforms.
90 VAC Input.
5 V_{PK-PK}: 28 mV, 12 V_{PK-PK}: 73 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

Figure 112 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
5 V_{PK-PK}: 26 mV, 12 V_{PK-PK}: 80 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

12.5.2.3 50% Load

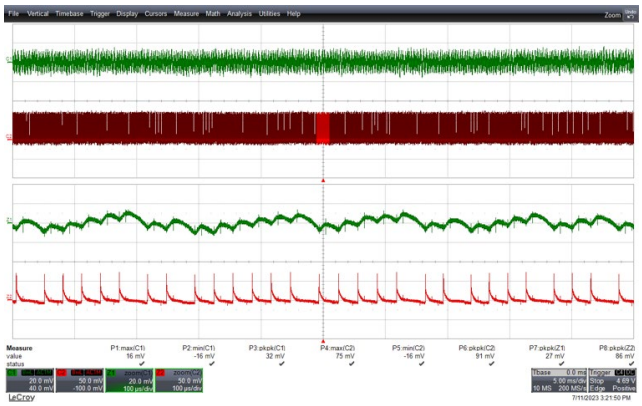


Figure 113 – Output Ripple Voltage Waveforms.
90 VAC Input.
5 V_{PK-PK}: 32 mV, 12 V_{PK-PK}: 91 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

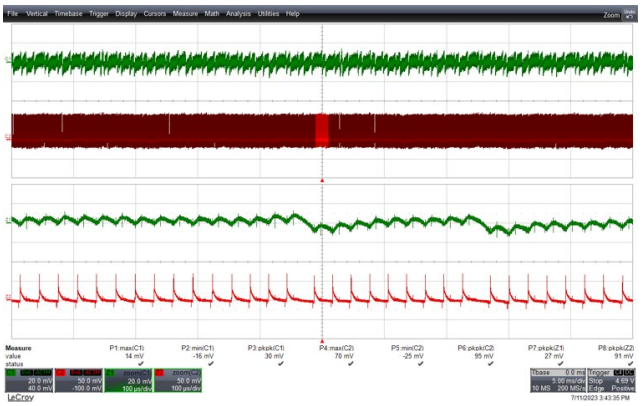


Figure 114 – Output Ripple Voltage Waveforms.
265 VAC Input.
5 V_{PK-PK}: 30 mV, 12 V_{PK-PK}: 95 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

12.5.2.4 75% Load

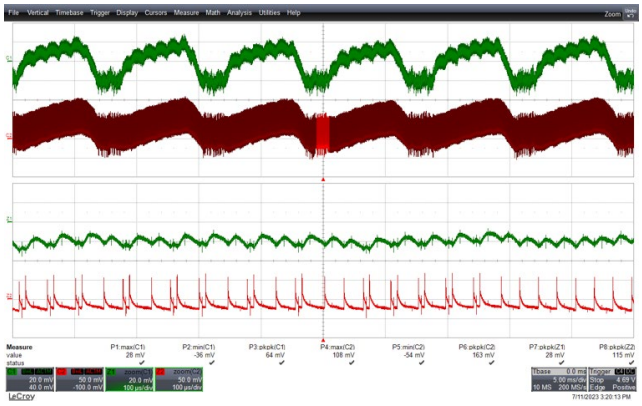


Figure 115 – Output Ripple Voltage Waveforms.
90 VAC Input.
5 V_{PK-PK}: 64 mV, 12 V_{PK-PK}: 163 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

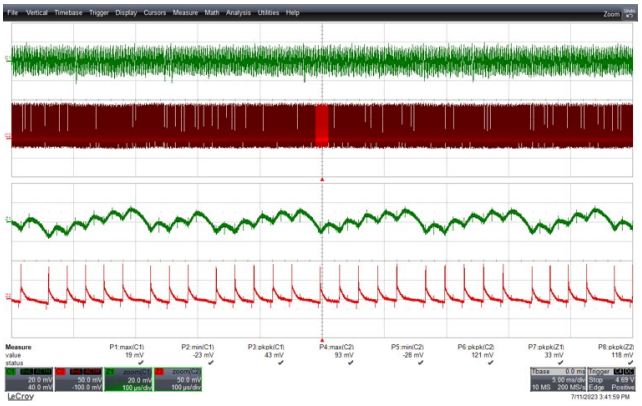


Figure 116 – Output Ripple Voltage Waveforms.
265 VAC Input.
5 V_{PK-PK}: 43 mV, 12 V_{PK-PK}: 121 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

12.5.2.5 100% Load

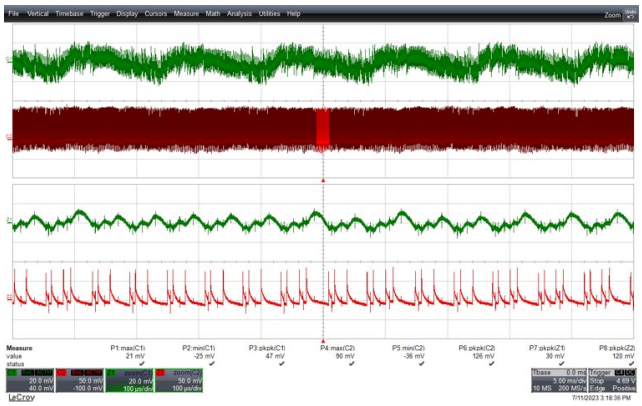


Figure 117 – Output Ripple Voltage Waveforms.
90 VAC Input.
5 V_{PK-PK}: 47 mV, 12 V_{PK-PK}: 126 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 μs / div.

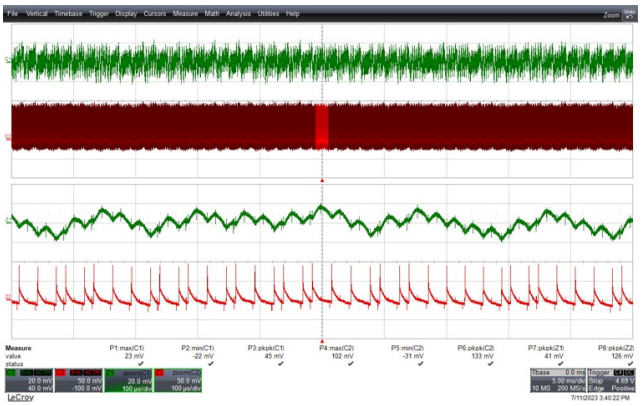


Figure 118 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
5 V_{PK-PK}: 45 mV, 12 V_{PK-PK}: 133 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 μs / div.

12.5.3 Ripple Voltage Waveforms (uVCC = 3.3 V / 20 mA)

Note: Both 5 V & 12 V output are loaded with the same percentage.

12.5.3.1 0% Load

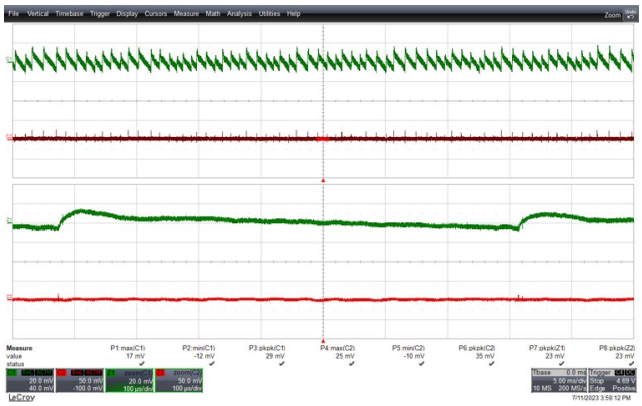


Figure 119 – Output Ripple Voltage Waveforms.
90 VAC Input.
5 V_{PK-PK}: 29 mV, 12 V_{PK-PK}: 35 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

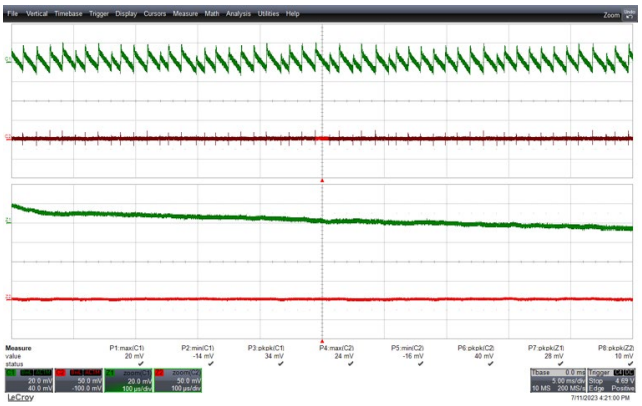


Figure 120 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
5 V_{PK-PK}: 34 mV, 12 V_{PK-PK}: 40 gd mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

12.5.3.2 25% Load

Figure 121 – Output Ripple Voltage Waveforms.
90 VAC Input.
5 V_{PK-PK}: 27 mV, 12 V_{PK-PK}: 76 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

Figure 122 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
5 V_{PK-PK}: 24 mV, 12 V_{PK-PK}: 81 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

12.5.3.3 50% Load

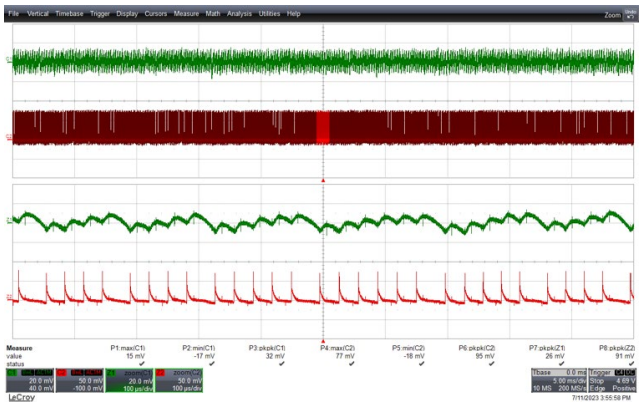


Figure 123 – Output Ripple Voltage Waveforms.
90 VAC Input.
5 V_{PK-PK}: 32 mV, 12 V_{PK-PK}: 95 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div..

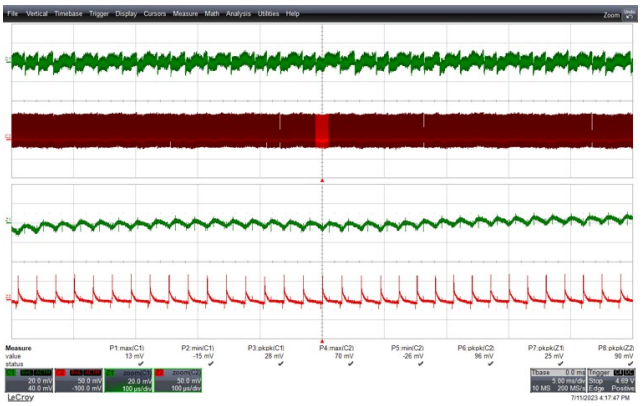


Figure 124 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
5 V_{PK-PK}: 28 mV, 12 V_{PK-PK}: 96 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

12.5.3.4 75% Load

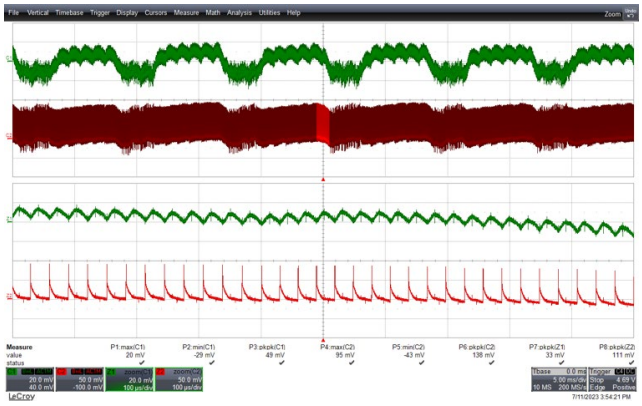


Figure 125 – Output Ripple Voltage Waveforms.
90 VAC Input.
5 V_{PK-PK}: 49 mV, 12 V_{PK-PK}: 138 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

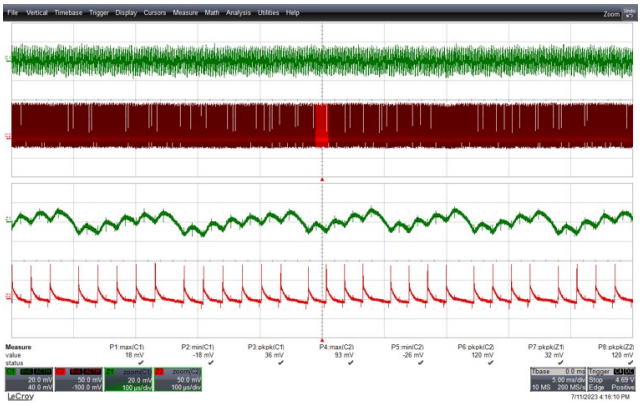


Figure 126 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
5 V_{PK-PK}: 36 mV, 12 V_{PK-PK}: 120 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 µs / div.

12.5.3.5 100% Load

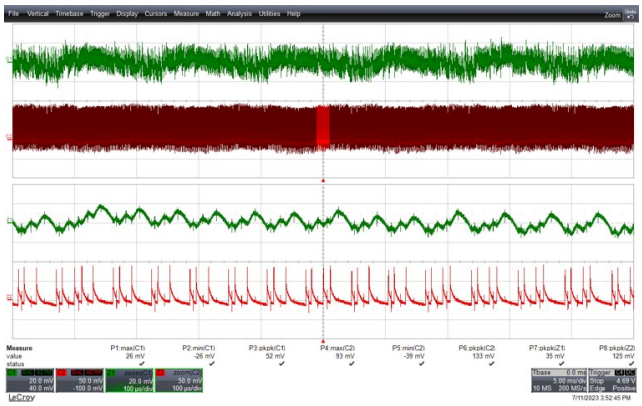


Figure 127 – Output Ripple Voltage Waveforms.
90 VAC Input.
5 V_{PK-PK}: 52 mV, 12 V_{PK-PK}: 133 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 μs / div.

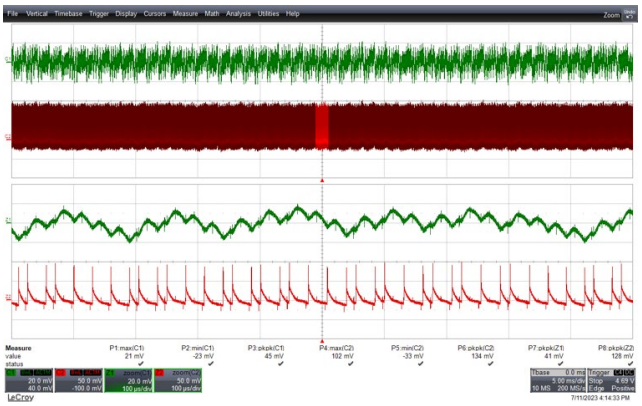


Figure 128 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
5 V_{PK-PK}: 45 mV, 12 V_{PK-PK}: 134 mV.
Upper: 5 V_{OUT}, 20 mV / div, 5 ms / div.
Lower: 12 V_{OUT}, 50 mV / div, 5 ms / div.
Zoom: 100 μs / div.

12.5.4 Ripple (ATE Measurements)

Note: Both 5 V & 12 V output are loaded with the same percentage.

12.5.4.1 5 V Output Ripple (uVCC = 3.3 V / 0 A)

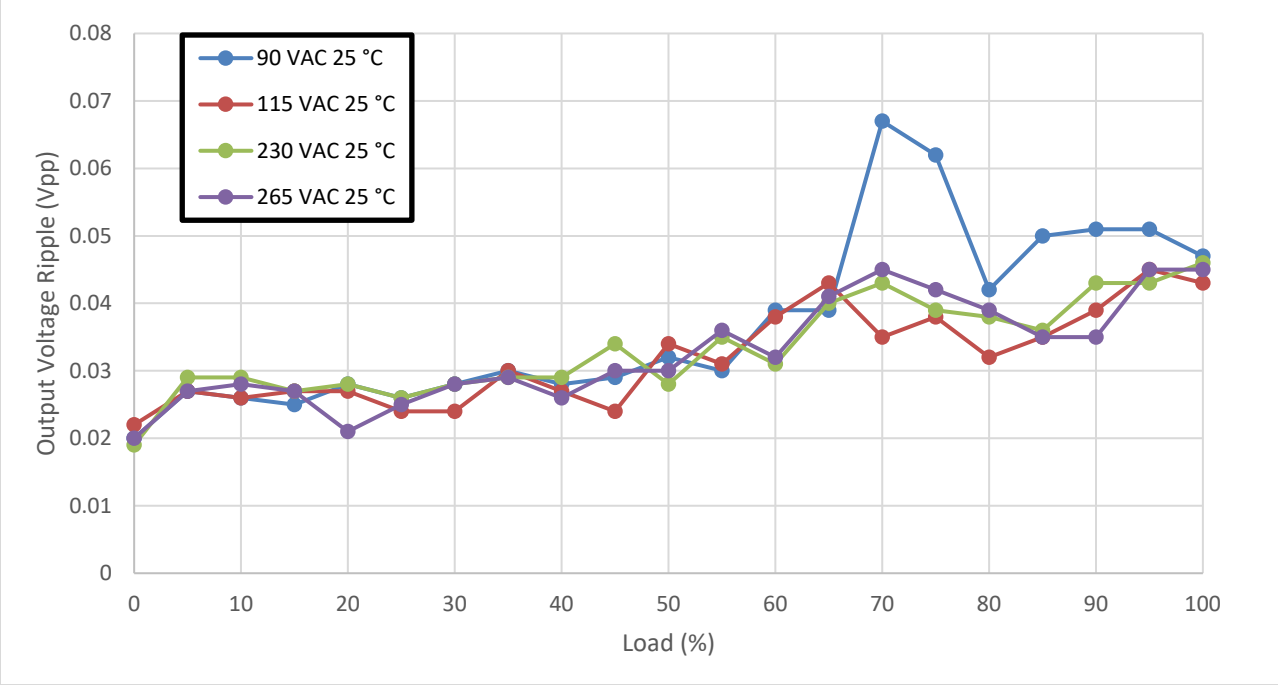


Figure 129 – 5 V Output Voltage Ripple vs. Output Load, Room Ambient – 25 ºC Temperature.

12.5.4.2 5 V Output Ripple (uVCC = 3.3 V / 20 mA)

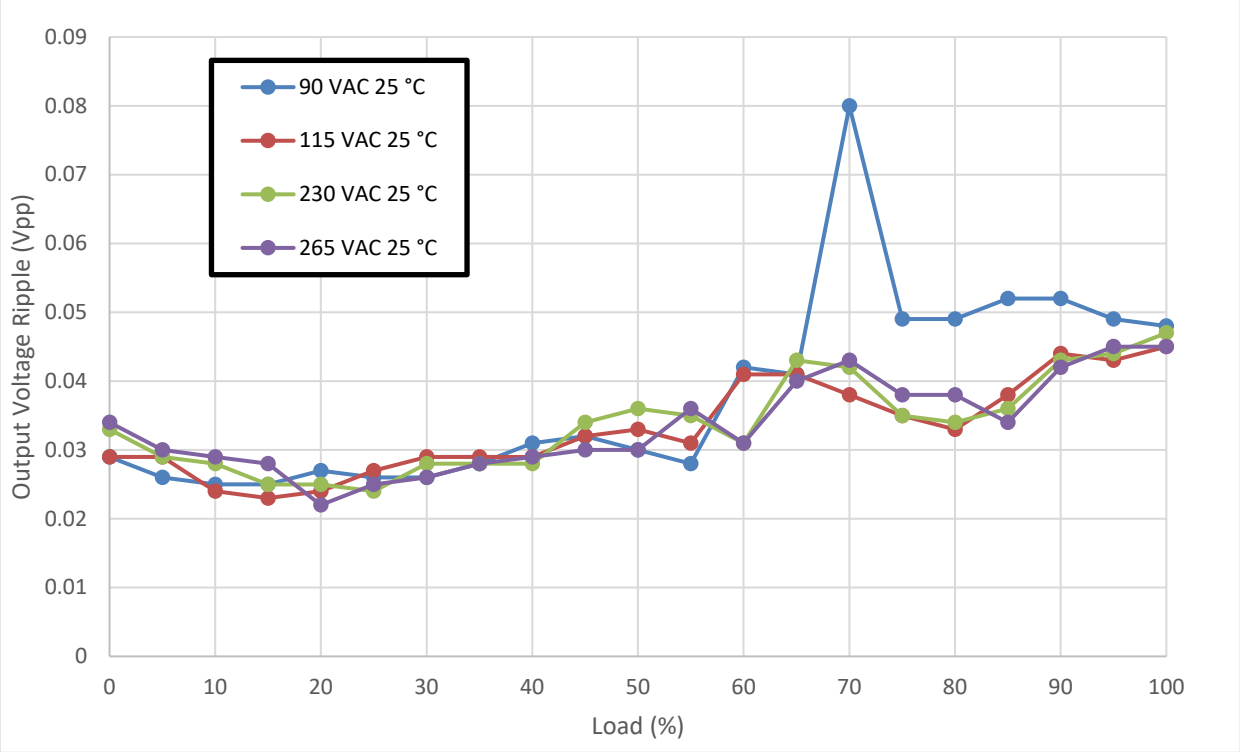


Figure 130 – 5 V Output Voltage Ripple vs. Output Load, Room Ambient – 25 ºC Temperature.

12.5.4.3 12 V Output Ripple (uVCC = 3.3 V / 0 A)

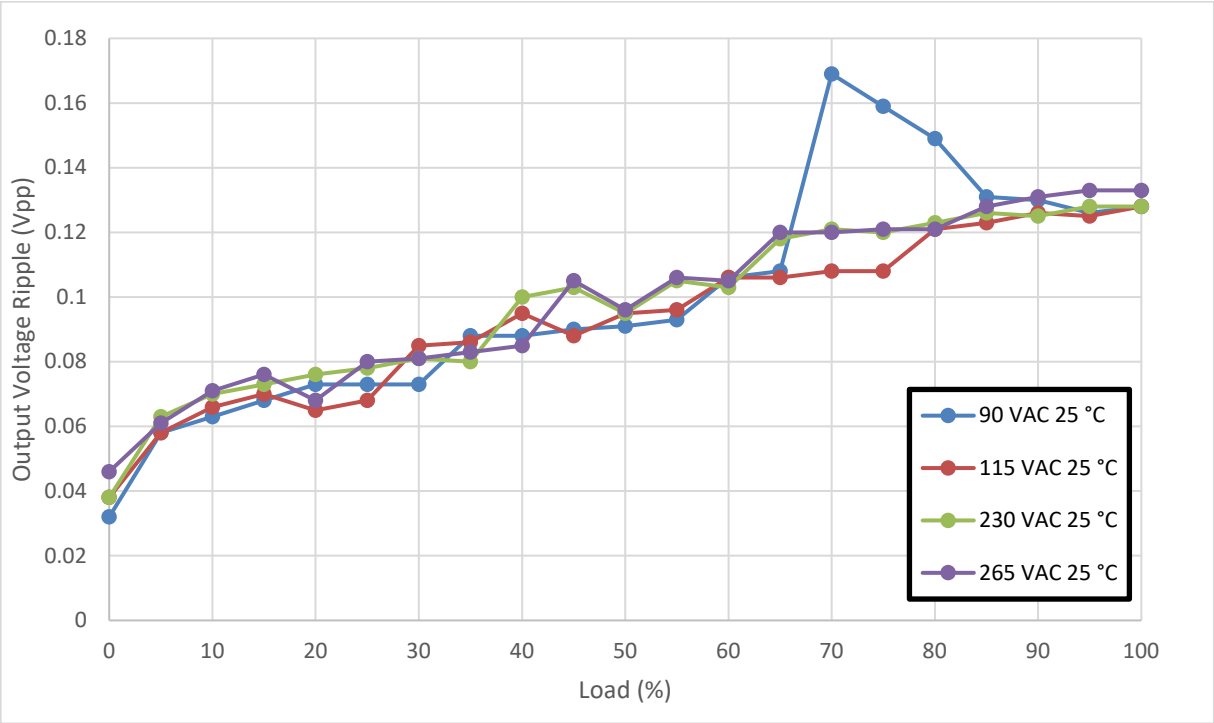


Figure 131 – 12 V Output Voltage Ripple vs. Output Load, Room Ambient – 25 ºC Temperature.

12.5.4.4 12 V Output Ripple (uVCC = 3.3 V / 20 mA)

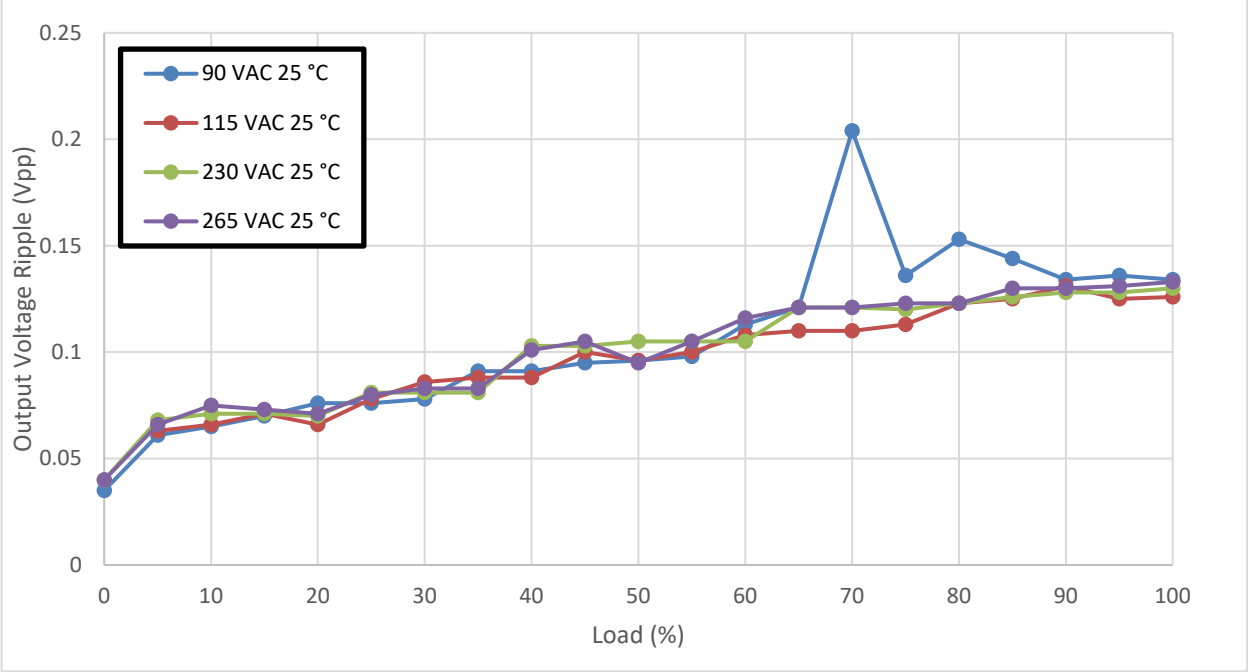


Figure 132 – 12 V Output Voltage Ripple vs. Output Load, Room Ambient – 25 ºC Temperature.

12.6 *Brown-In / Brown-Out Recovery Test*

No abnormal overheating or voltage overshoot / undershoot was observed. The unit works normally after the brown-out test.

12.6.1 5 V / 1.4 A & 12 V / 0.42 A Output, uVCC = 3.3 V / 0 A

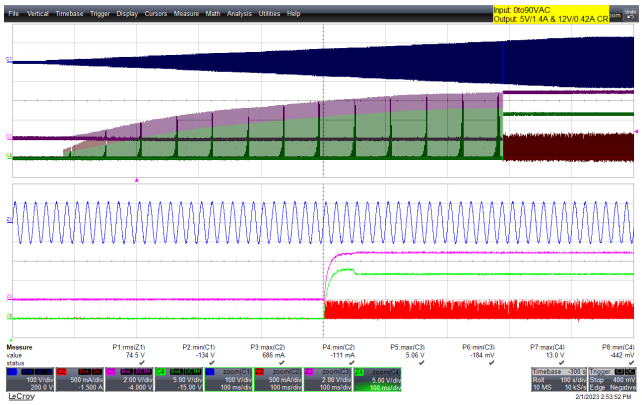


Figure 133 – Brown-In Waveforms.
0 to 90 VAC Input, Full Load.
Upper: AC Input, 100 V / div.
Upper Middle: 5 V_{OUT}, 2 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 500 mA / div.
100 s / div.
Zoom: 100 ms / div.
Brown-In Voltage = 74.5 VAC.

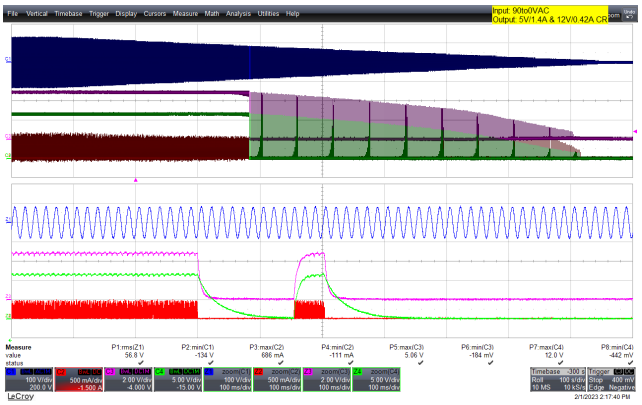


Figure 134 – Brown-Out Waveforms.
90 to 0 VAC Input, Full Load.
Upper: AC Input, 100 V / div.
Upper Middle: 5 V_{OUT}, 2 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 500 mA / div.
100 s / div.
Zoom: 100 ms / div.
Brown-Out Voltage = 56.8 VAC.

12.6.2 5 V / 1.4 A & 12 V / 0.42 A Output, uVCC = 3.3 V / 20 mA

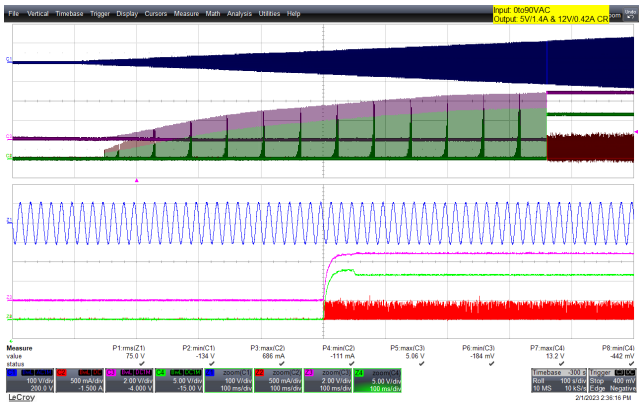


Figure 135 – Brown-In Waveforms.
0 to 90 VAC Input, Full Load.
Upper: AC Input, 100 V / div.
Upper Middle: 5 V_{OUT}, 2 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 500 mA / div.
100 s / div.
Zoom: 100 ms / div.
Brown-In Voltage = 75 VAC.

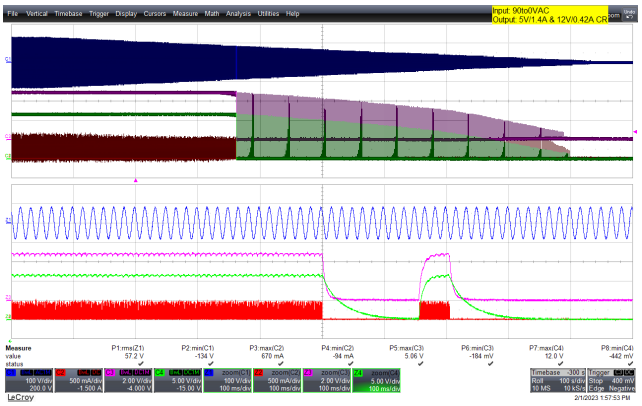


Figure 136 – Brown-Out Waveforms.
90 to 0 VAC Input, Full Load.
Upper: AC Input, 100 V / div.
Upper Middle: 5 V_{OUT}, 2 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 500 mA / div.
100 s / div.
Zoom: 100 ms / div.
Brown-Out Voltage = 57.2 VAC.

12.6.3 5 V / 0 A & 12 V / 0 A Output, uVCC = 3.3 V / 0 A

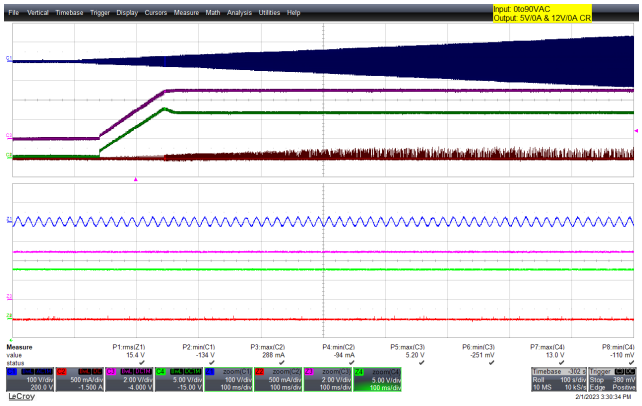


Figure 137 – Brown-In Waveforms.
0 to 90 VAC Input, No-Load.
Upper: AC Input, 100 V / div.
Upper Middle: 5 V_{OUT}, 2 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 500 mA / div.
100 s / div.
Zoom: 100 ms / div.
Brown-In Voltage = 15.4 VAC.

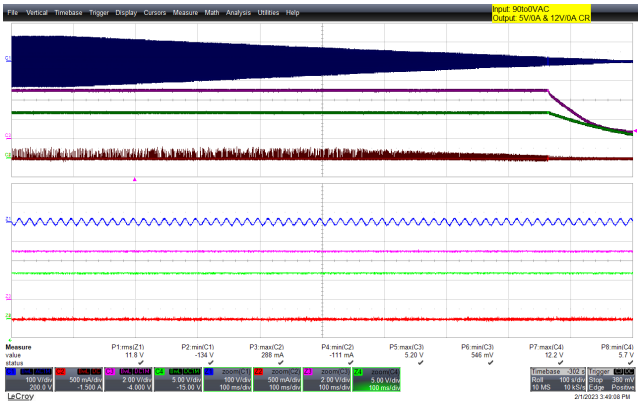


Figure 138 – Brown-Out Waveforms.
90 to 0 VAC Input, No-Load.
Upper: AC Input, 100 V / div.
Upper Middle: 5 V_{OUT}, 2 V / div.
Lower Middle: 12 V_{OUT}, 5 V / div.
Lower: LNK-XT2SR_I_{DS}, 500 mA / div.
100 s / div.
Zoom: 100 ms / div.
Brown-Out Voltage = 11.8 VAC.

13 EMI

13.1 *Conductive EMI*

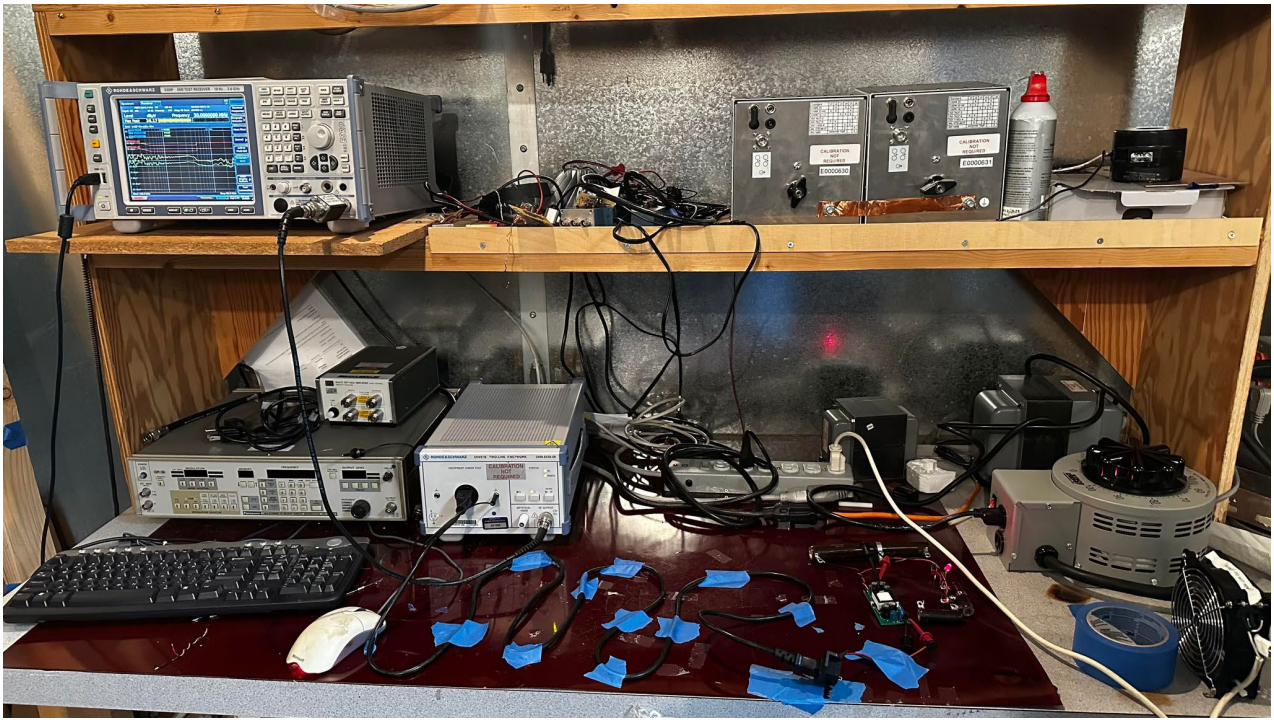


Figure 139 – EMI Test Set-up.

13.1.1 Floating Output (QP / AV)

13.1.1.1 115 VAC Input (uVCC = 3.3 V / 0 A)

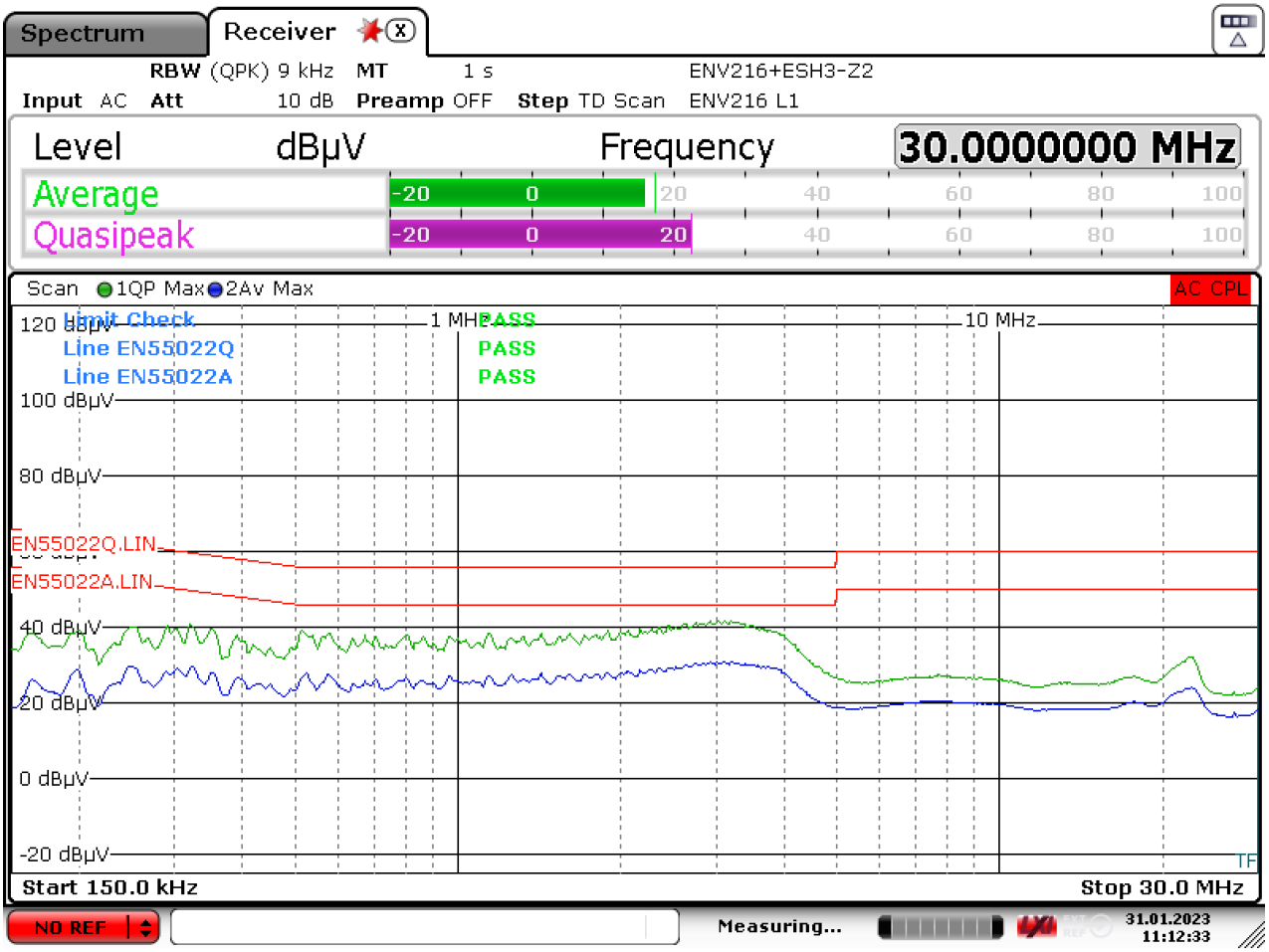


Figure 140 – Floating Output - 115 VAC Line.

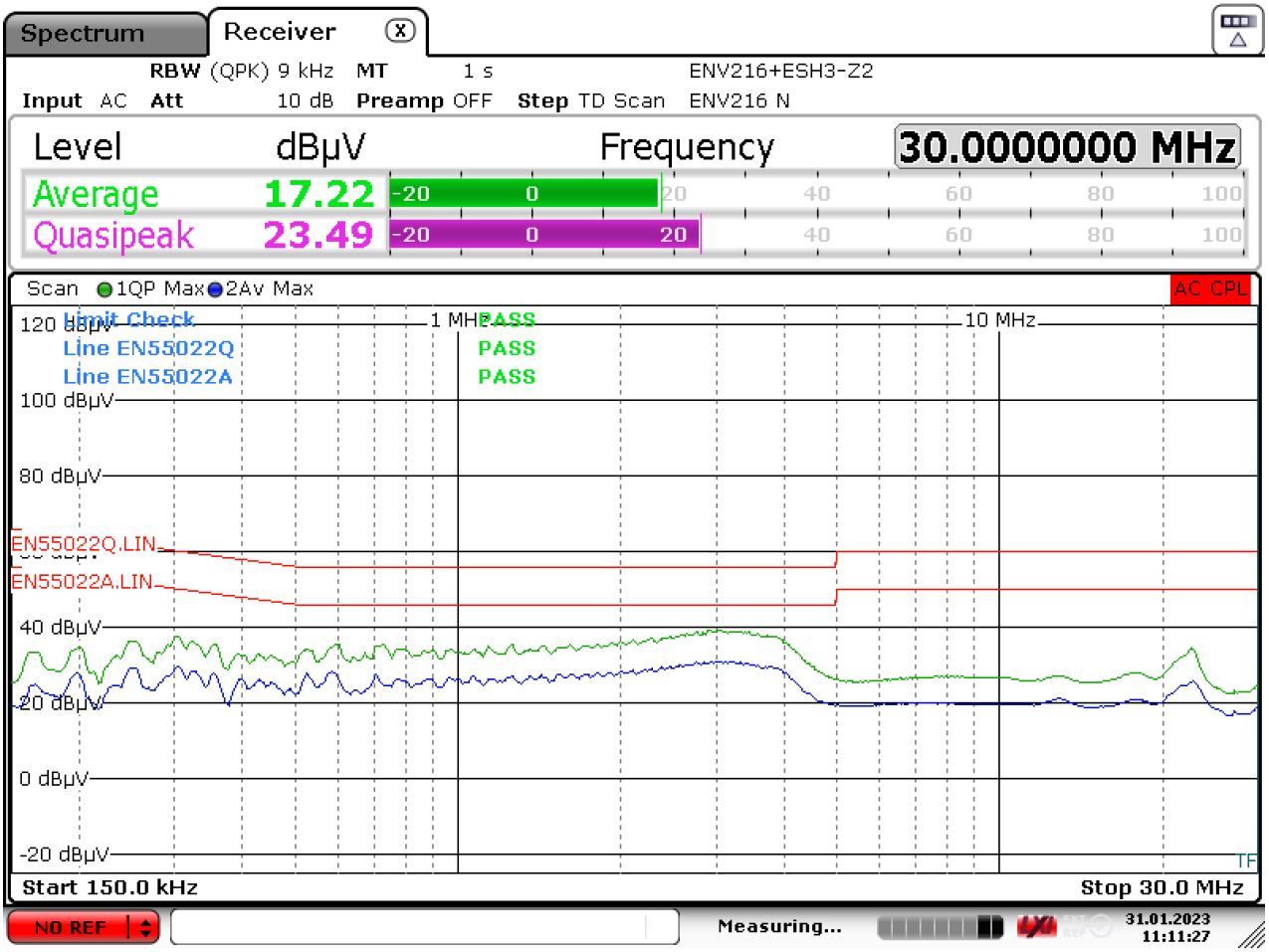


Figure 141 – Floating Output - 115 VAC Neutral.

13.1.1.2 115 VAC Input (uVCC = 3.3 V / 20 mA)

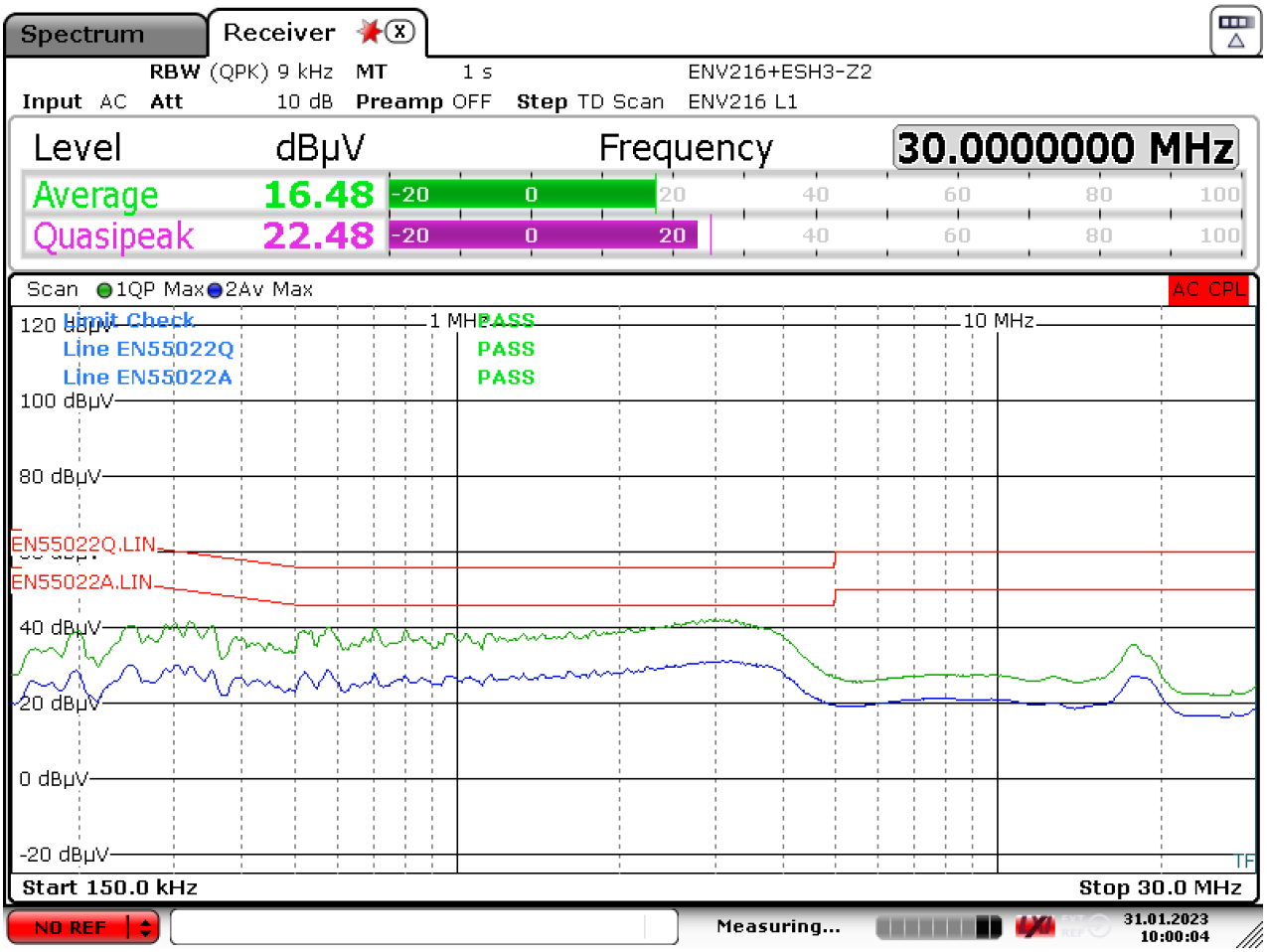


Figure 142 – Floating Output - 115 VAC Line.

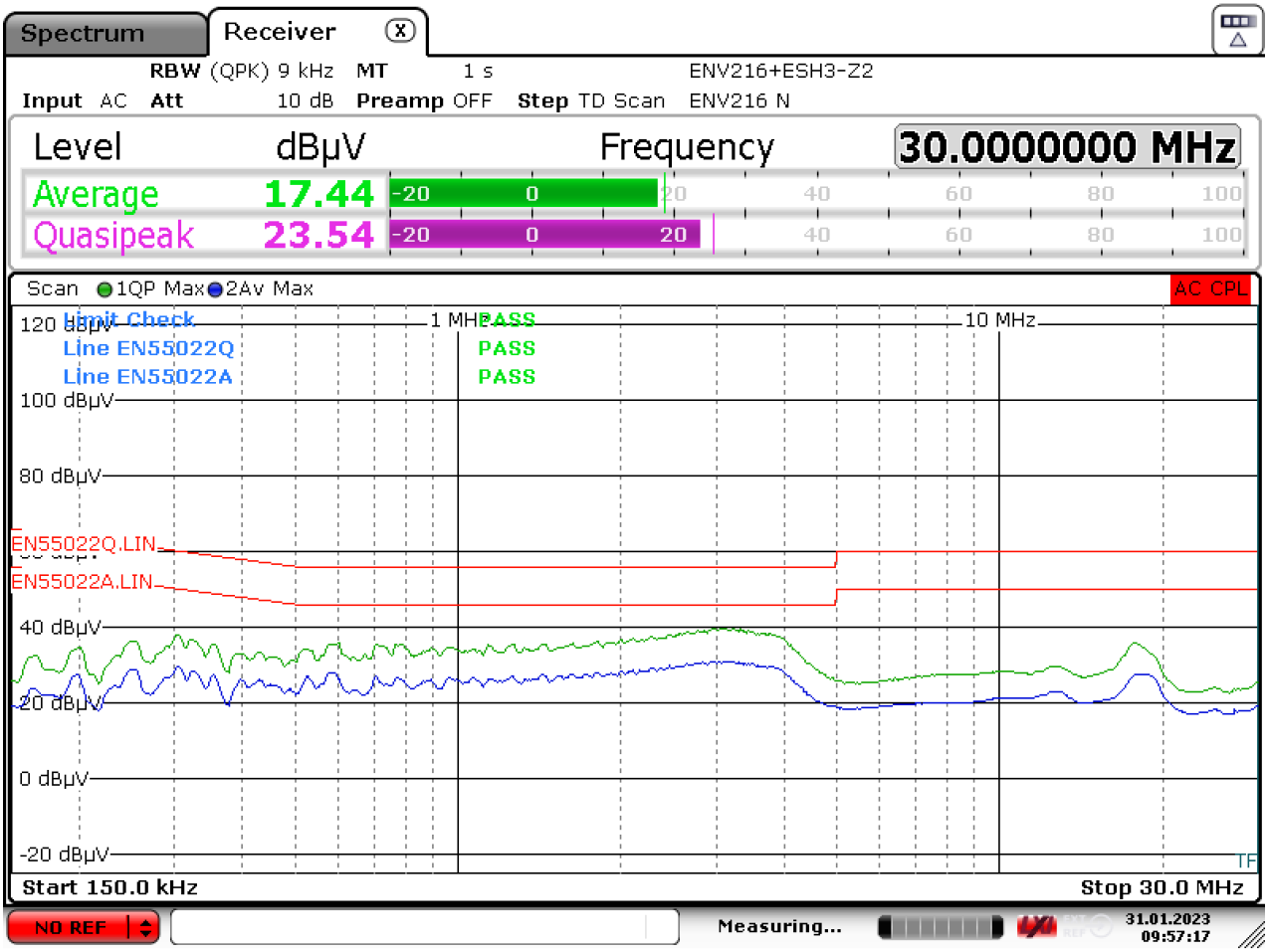


Figure 143 – Floating Output - 115 VAC Neutral.

13.1.1.3 230 VAC Input (uVCC = 3.3 V / 0 A)

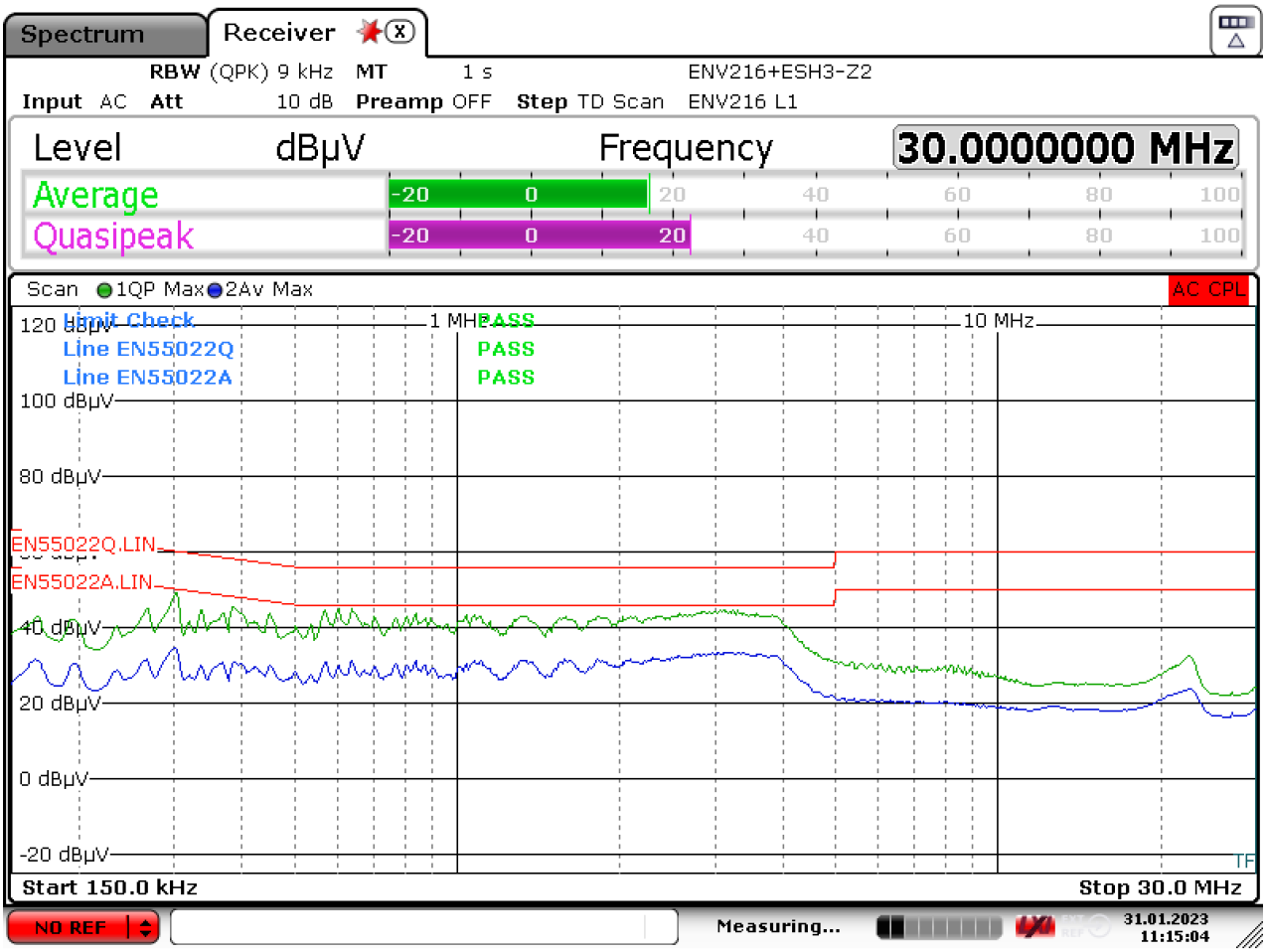


Figure 144 – Floating Output - 230 VAC Line.

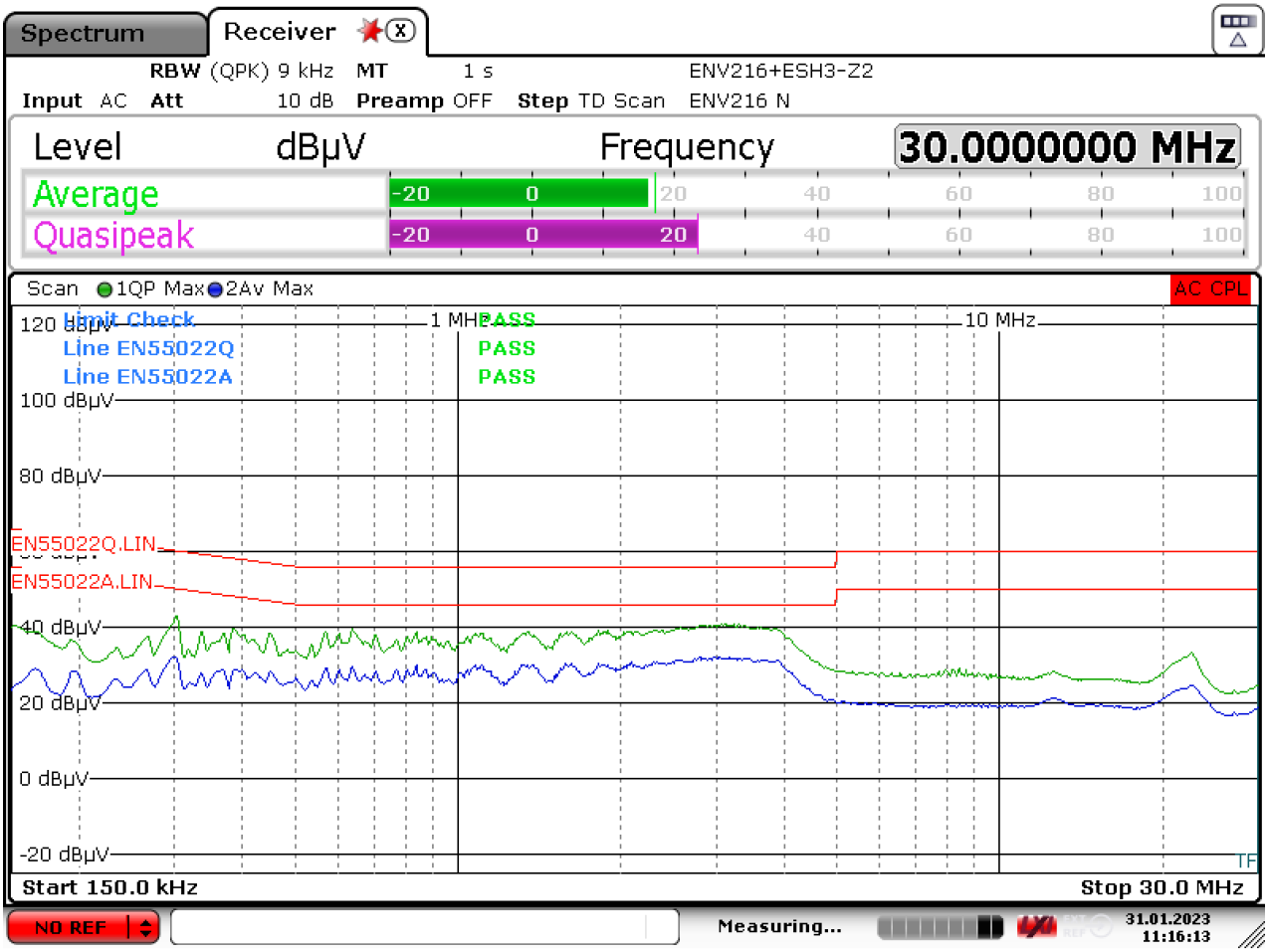


Figure 145 – Floating Output - 230 VAC Neutral.

13.1.1.4 230 VAC Input (uVCC = 3.3 V / 20 mA)

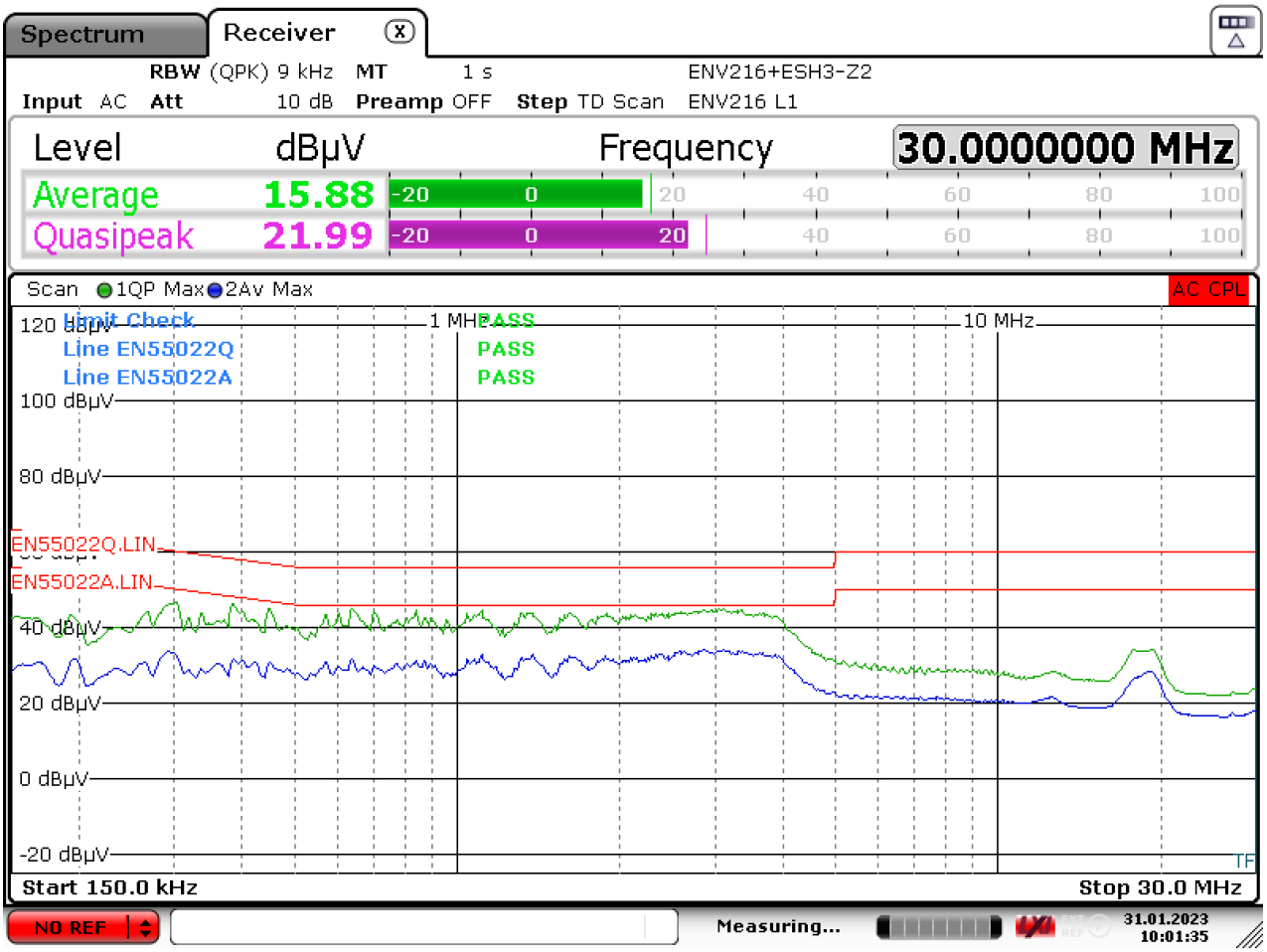


Figure 146 – Floating Output - 230 VAC Line.

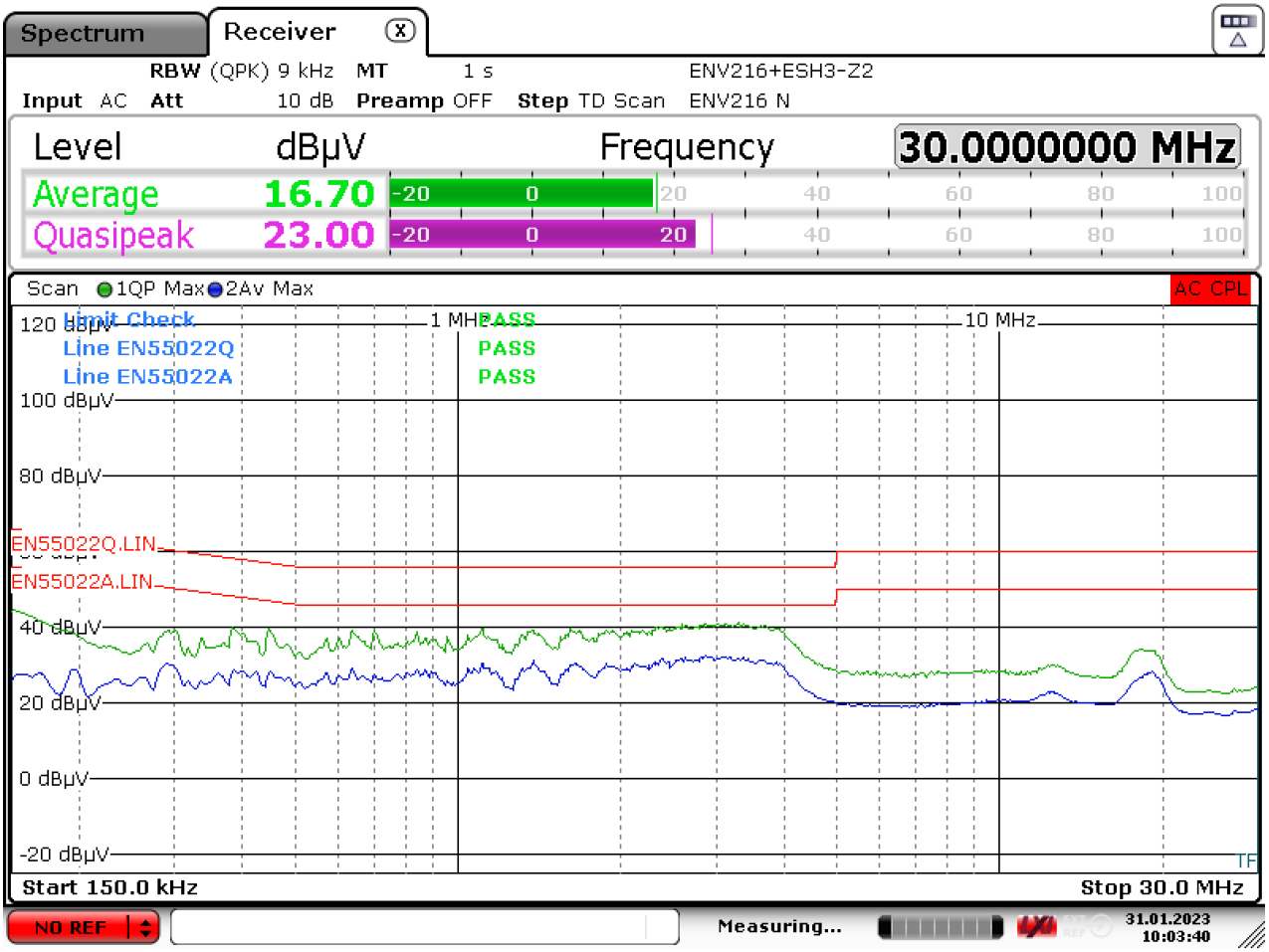


Figure 147 – Floating Output - 230 VAC Neutral.

14 Line Immunity

Output Load set at maximum load (5 V / 1.4 A & 12 V / 0.42 A).

- Using 3.57 Ω fixed resistor for 5 V output.
- Using 28.57 Ω fixed resistor for 12 V output.

14.1 *Differential Surge Test Results*

Repetition rate: 1 strike / 30 seconds
Passed ±1 kV, 500 A surge test.

Surge Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Test Result
1	0	L, N	2	10	PASS
-1	0	L, N	2	10	PASS
1	90	L, N	2	10	PASS
-1	90	L, N	2	10	PASS
1	180	L, N	2	10	PASS
-1	180	L, N	2	10	PASS
1	270	L, N	2	10	PASS
-1	270	L, N	2	10	PASS

Figure 148 – 230 VAC, +1 kV, Differential Surge L-N

Injection Phase: 90°.
Upper: V_{BULK}, 200 V / div.
Lower: V_{DRAIN}, 200 V / div. Max V_{DS} = 638 V.
1 ms / div.
Zoom: 50 µs / div.

14.2 *Ring Wave Surge Test Results*

Repetition rate: 1 strike / 30 seconds

Passed ±6 kV, ring wave test.

Ring Wave Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Test Result
2	0	L, N	12	10	PASS
-2	0	L, N	12	10	PASS
2	90	L, N	12	10	PASS
-2	90	L, N	12	10	PASS
2	180	L, N	12	10	PASS
-2	180	L, N	12	10	PASS
2	270	L, N	12	10	PASS
-2	270	L, N	12	10	PASS
4	0	L, N	12	10	PASS
-4	0	L, N	12	10	PASS
4	90	L, N	12	10	PASS
-4	90	L, N	12	10	PASS
4	180	L, N	12	10	PASS
-4	180	L, N	12	10	PASS
4	270	L, N	12	10	PASS
-4	270	L, N	12	10	PASS
6	0	L, N	12	10	PASS
-6	0	L, N	12	10	PASS
6	90	L, N	12	10	PASS
-6	90	L, N	12	10	PASS
6	180	L, N	12	10	PASS
-6	180	L, N	12	10	PASS
6	270	L, N	12	10	PASS
-6	270	L, N	12	10	PASS

14.3 **EFT**

Tested at 5 kHz and 100 kHz EFT Burst frequency with test duration of 120 s. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

Passed ±2 kV, EFT test.

EFT Surge Voltage (kV)	Phase Angle (°)	IEC Coupling	Frequency	T-Burst	T-Rep	Test Result
2	0	L, N	5 kHz	15 ms	300 ms	PASS
-2	0	L, N	5 kHz	15 ms	300 ms	PASS
2	90	L, N	5 kHz	15 ms	300 ms	PASS
-2	90	L, N	5 kHz	15 ms	300 ms	PASS
2	180	L, N	5 kHz	15 ms	300 ms	PASS
-2	180	L, N	5 kHz	15 ms	300 ms	PASS
2	270	L, N	5 kHz	15 ms	300 ms	PASS
-2	270	L, N	5 kHz	15 ms	300 ms	PASS
2	0	L, N	100 kHz	750 μs	300 ms	PASS
-2	0	L, N	100 kHz	750 μs	300 ms	PASS
2	90	L, N	100 kHz	750 μs	300 ms	PASS
-2	90	L, N	100 kHz	750 μs	300 ms	PASS
2	180	L, N	100 kHz	750 μs	300 ms	PASS
-2	180	L, N	100 kHz	750 μs	300 ms	PASS
2	270	L, N	100 kHz	750 μs	300 ms	PASS
-2	270	L, N	100 kHz	750 μs	300 ms	PASS

15 Revision History

Date	Author	Revision	Description & Changes	Reviewed
12-Sep-23	MA	1.0	Initial Release.	Apps & Mktg

For the latest updates, visit our website: www.power.com

Reference Designs are technical proposals concerning how to use Power Integrations' gate drivers in particular applications and/or with certain power modules. These proposals are "as is" and are not subject to any qualification process. The suitability, implementation and qualification are the sole responsibility of the end user. The statements, technical information and recommendations contained herein are believed to be accurate as of the date hereof. All parameters, numbers, values and other technical data included in the technical information were calculated and determined to our best knowledge in accordance with the relevant technical norms (if any). They may base on assumptions or operational conditions that do not necessarily apply in general. We exclude any representation or warranty, express or implied, in relation to the accuracy or completeness of the statements, technical information and recommendations contained herein. No responsibility is accepted for the accuracy or sufficiency of any of the statements, technical information, recommendations or opinions communicated and any liability for any direct, indirect or consequential loss or damage suffered by any person arising therefrom is expressly disclaimed.

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

Patent Information
The products and applications illustrated herein (including transformer construction and circuits' external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.power.com/ip.htm.

Power Integrations, the Power Integrations logo, CAPZero, ChiPhy, CHY, DPA-Switch, EcoSmart, E-Shield, eSIP, eSOP, HiperPLC, HiperPFS, HiperTFS, InnoSwitch, Innovation in Power Conversion, InSOP, LinkSwitch, LinkZero, LYTSwitch, SENZero, TinySwitch, TOPSwitch, PI, PI Expert, PowiGaN, SCALE, SCALE-1, SCALE-2, SCALE-3 and SCALE-iDriver, are trademarks of Power Integrations, Inc. Other trademarks are property of their respective companies. ©2019, Power Integrations, Inc.

Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

CHINA (SHANGHAI)
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

CHINA (SHENZHEN)
17/F, Hivac Building, No. 2, Keji Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

GERMANY (AC-DC/LED Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

GERMANY (Gate Driver Sales)
HellwegForum 1
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

JAPAN
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com